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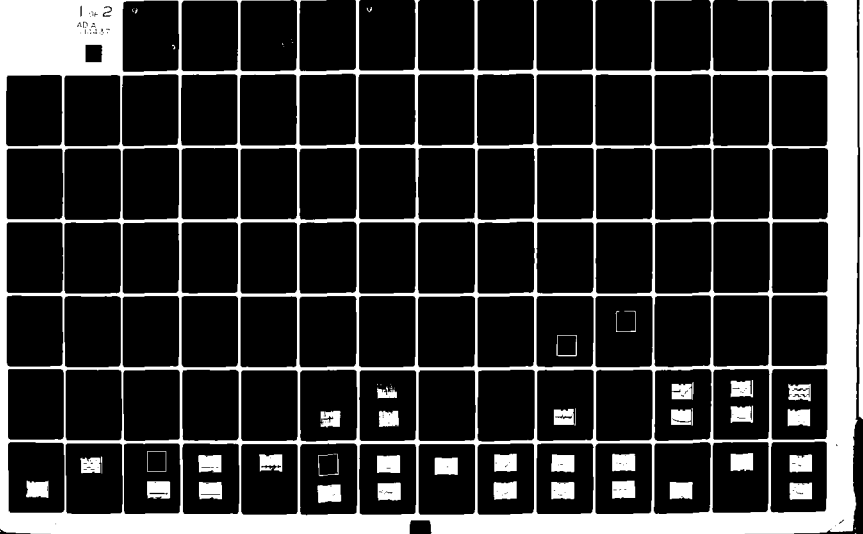

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Research and Development Technical Report

DELET-TR-80-0302
Technical Guidelines For LSI Hybrid Microcircuits

R. Rego
C. Ross

RAYTHEON COMPANY
MISSILE SYSTEMS DIVISION
BEDFORD, MASSACHUSETTS

1 April 1982

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Prepared For
Electronics Technology and Device Laboratory

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

THIS REPORT DESCRIBES THE STATUS OF THE WORK DONE DURING THE INITIAL PHASE OF THE CONTRACT TO DEVELOP DESIGN AND LAY-OUT RULES WHICH CAN BE USED AS A DATA BASE FOR THE COMPUTER AIDED INTERCONNECTION DESIGN OF DIGITAL HYBRID MICROCIRCUITS. A REQUIREMENT IS THE USE OF EXISTING OR NEAR TERM PRODUCTION DEVICES OF SELECTED SEMICONDUCTOR TECHNOLOGIES THAT OPERATE AT CLOCK RATES FROM 10 to 250 MHz WITH SWITCHING SPEEDS UP

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TO 1 GHz. DURING THIS PERIOD VARIOUS COMPUTER SIMULATION PROGRAMS WERE EVALUATED AND RAYCAP, A REFORMATTED VERSION OF THE AEDCAP PROGRAM PURCHASED FROM SOFTECH INC., WAS SELECTED TO GENERATE SIMULATION OF CASCADED LUMPED PARAMETER CIRCUIT MODELS. THE ACCURACY OF THE CASCADE LUMPED PARAMETER PROGRAM WAS VERIFIED BY A COMPREHENSIVE NETWORK OF SIMULATION PROBLEMS THAT WERE COMPARED TO CALCULATED SOLUTIONS. THE LSI/VLSI DEVICE FAMILIES SELECTED INCLUDED STTL, LSTTL, COS/MOS AND ECL BASED ON READILY AVAILABLE CHIPS THAT MEET THE PROGRAMS CLOCK RATE AND SPEED REQUIREMENTS. A STUDY TO DETERMINE THE THERMAL CONSTRAINTS THAT MAY AFFECT THE DENSE PACKAGING OF DEVICES IN HERMETIC CHIP CARRIERS HAS BEEN COMPLETED IN ADDITION TO A COMPLIMENTARY STUDY USING CHIP AND WIRE DEVICES ON THICK FILM SUBSTRATES. THICK FILM, MULTILAYER HYBRID TEST SUBSTRATES THAT CONTAIN VARIOUS LINE WIDTHS, SPACINGS AND BENDS WITH NO ACTIVE DEVICES HAVING BEEN CHARACTERIZED USING TIME DOMAIN REFLECTOMETRY AND PULSE RESPONSE MEASUREMENTS. THICK FILM, MULTILAYER HYBRID CIRCUITS THAT CONTAIN CMOS/SOS,LSTTL, STTL, AND ECL DEVICES HAVE BEEN TESTED AND CHARACTERIZED USING TIME DOMAIN REFLECTOMETRY AND PULSE RESPONSE MEASUREMENT.

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1. INTRODUCTION AND SUMMARY

The primary objective of this program is to develop design and layout rules which can be used as a data base for the Computer Aided Interconnection design of digital hybrid circuits. A requirement is the use of existing or near term production Large Scale Integration (LSI)/Very Large Scale Integration (VLSI) devices of selected semiconductor technologies that operate at clock rates from 10 to 250 MHz with switching speeds up to 1 GHz. An additional requirement is that the substrate interconnect packaging design will employ mainstream, high production throughput technology. Therefore, primary emphasis is given to developing a high density interconnect design that delays the need for transmission line technology over the frequency range of interest. To accomplish this objective the hybrid technology features short inter-chip connections and high density multilayering. This approach achieves low capacitance interconnects, thereby reducing drive power and signal propagation delay. In some applications, high density interconnects will not preserve the signals communicating between chips across the entire frequency span of interest. Therefore, the crossover conditions where the interconnect must be treated as a lumped element and where it must be treated as a transmission line are analytically and experimentally determined. The design rules generated by this program are to be verified by the design, fabrication, test and evaluation of functional demonstration units which feature standard interconnect designs that transverse from simple to lumped to transmission line technology.

The program status is as follows: Various computer circuit simulation programs were evaluated and a Raytheon program (RAYCAP) was selected. RAYCAP is a reformatted version of the AEDCAP Program which was purchased by Raytheon from Softech Inc. Since it is interactive, it generates fast turn around simulations in an accurate pulse response form.

Both transmission line and cascaded lumped parameter circuit models were evaluated using RAYCAP. Since the transmission line model is a lossless model, rather than a lossy model, it was rejected. The accuracy of the cascade lumped parameter program was verified by a comprehensive network of simulation problems that were compared to calculated solutions.

A survey of candidate LSI/VLSI device families have been completed. Four circuit families were selected: STTL, LSTTL, Complimentary Metal Oxide Semiconductor (CMOS)/Silicon on Sapphire (SOS) and Emitter Coupled Logic (ECL). The selection is based on readily available chips that meet the programs clock rate and speed requirements. A study to determine the thermal constraints that may affect the dense packaging of devices in hermetic chip carriers has been completed in addition to a complimentary study using Chip and Wire Devices on thick film substrates.

Thick film, mutilayer hybrid test substrates that contain various line widths, spacings and bends with no active devices have been characterized using Time Domain Reflectometry (TDR) and pulse response measurements.

Also, thick film functional circuits built with high density, simple interconnect, microstrip and stripline technology have been fabricated and are now in test evaluation. These functional test hybrids are devices of the four selected families packaged in hermetic chip carriers as well as Chip and Wire.

Based upon the above analyses and measurements, a determination of where simple interconnect microstrip or transmission line technology is needed will be made for each of the device families.

A set of preliminary simplified design rules that can be incorporated into a Computer Aided Design (CAD) program will be generated. To prove the validity of the design rules, an additional set of hybrids will be designed, built and tested.

2. SIMULATION PROGRAMS

A survey of computer programs that could be used to simulate digital circuits and hybrid interconnects was performed. Based on the survey a computer simulation program that would best fit the needs of the task was selected. A simulation of an interconnect type, whose pulse response fits classic transmission theory, was performed and the results compared to predicted and calculated results.

2.1 Candidate Computer Programs

1) COMPAC - Computer Optimization of Microwave Passive and Active Circuits, Compact Engineering Inc., Los Altos, CA.
2) AEDCAP - Automated Engineering Design Circuit Analysis Program, Softech, Waltham, MA (Program developed at University of California).
3) RAYCAP, Raytheon Circuit Analysis Program (reformatted and enhanced AEDCAP), Raytheon Co., Bedford, MA.
4) Spice II - Simulation Program with Integrated Circuit Emphasis, University of California, Berkley, CA.

COMPAC - The input parameters to this program must be in the form of "S" parameters. The output parameters are in "S" parameters also. What is required is the time/pulse response of the circuit.

AEDCAP - This circuit analysis program does provide the desired pulse response as an output. However, simulations were very expensive as programs had to run, on a time share base, with an outside computer.

RAYCAP - AEDCAP rights were purchased and the program reformatted and enhanced and made interactive for very fast turnaround. It is for this reason that RAYCAP was selected. Spice II is very similar to AEDCAP and RAYCAP. The basic difference lies in the program language, not the user language. AEDCAP and RAYCAP are written in AED, while Spice II is written in the more familiar Fortran. Since Spice II is not interactive and

turnaround time is very long, possibly hours, it was rejected. However, in the future Spice II may be enhanced and made interactive by Raytheon, since conversion from RAYCAP to Spice II is a relatively easy task.

2.2 Interconnect Model

Both Spice II and RAYCAP have a built in transmission line model. A complete interconnect or segments of any interconnect can be described as a black box. The problem is that the model is lossless. Since some hybrid interconnects can be very lossy, especially thin film, this model was rejected. The approach selected is to represent a transmission line by cascaded RLC sections. Four sections, each representing one centimeter, make up the model. This representation is shown in Figure 2-1.

2.2.1 Model Validation

In order to validate the model a simulation was selected whose response could be accurately predicted. A source terminated line was used because it has an unusual response that is well documented in transmission line theory texts. Also, two different line delays are evident. When a transmission line is driven by a voltage source whose output impedance is equal to the characteristic impedance of the line, it is said to be source terminated. The response of the line is well defined and unique if the rise and fall time of the pulse at the source is less than the electrical delay of the line.

The voltage at the source impedance initially rises to one-half of the input voltage because the source impedance of the line forms a voltage divider. At the open or unterminated end of the line, one propagation delay later, the pulse edge arrives. The voltage reflects at full amplitude, and full voltage appears at the output. The reflected wavefront from the open end of the line arrives at the source another line delay later, bringing the voltage at the source impedance to full amplitude. At the source end of line the voltage goes to one half amplitude and stays there until two line delays later at which time it reaches full amplitude. This is shown graphically in Figure 2-2.

- 4 CM LINE
- CAN BE CASCADED
- CAN BE PARALLELED

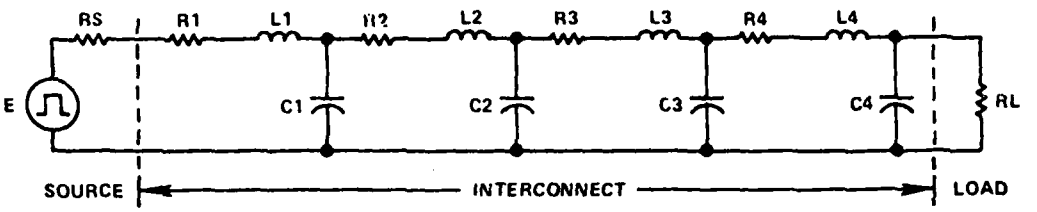
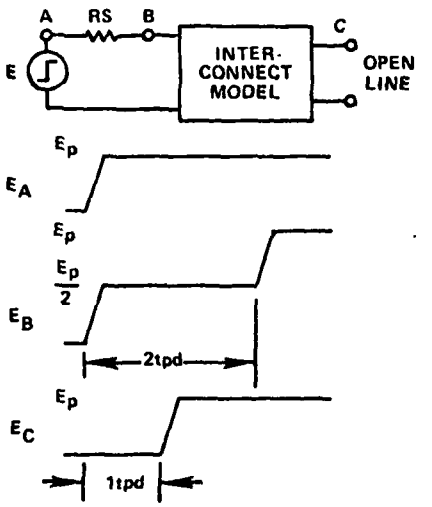


Figure 2-1 - Cascaded Lumped Parameter Model



$RS = Z_o$

WHERE Z_o = CHARACTERISTIC IMPEDANCE OF LINE

FOR 2 tpd $E_B = \frac{E_p Z_o}{R_s + Z_o} = \frac{E_p}{2}$

AT 1 tpd $E_c = \frac{E_p}{2} + \frac{E_p}{2} = E_p$

pd = propagation delay

Figure 2-2 - Classic Response of Source Terminated Line

To validate the model a source terminated microstrip interconnect was simulated. The interconnect was 4 cm long and 254 μm (10 mils) wide. The interconnect was on a 635 μm (25 mils) thick ceramic substrate with a power plane on the bottom. This microstrip configuration is depicted in Figure 2-3. The parameters required for the model were calculated using the formulas given in References 1 and 2. The calculations are shown in Figure 2-4.

The coding for the RAYCAP simulation is given in Figure 2-5. The simulation plot is shown in Figure 2-6. The responses E_B and E_C are as predicted. E_B does not attain full amplitude until two line delays later while E_C reaches full amplitude one line delay later. The simulations therefore agree with the analytical evaluation.

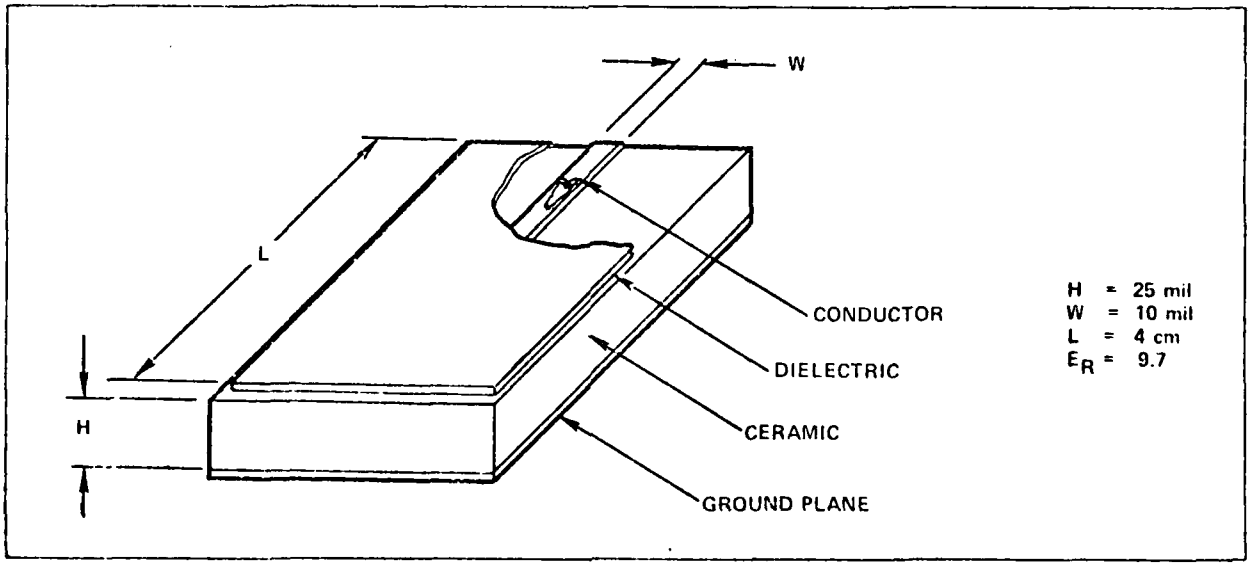


Figure 2-3 - Mircrostrip Interconnect

(1)

$$Z_o = \frac{60}{\sqrt{0.475\ \Sigma_r + 0.67}} \ln \frac{4h}{0.67\ (0.8\ w+t)}$$

Where: h = 25 mils = 0.0635 cm
w = 10 mils = 0.0254 cm
t = 0.8 mils = 0.002 cm
Σ_r = 9.7

(2)

$$\Sigma_{reff} = \frac{\Sigma r + 1}{2} + \frac{\Sigma r - 1}{2} \frac{1}{\sqrt{1 + \frac{10h}{w}}} \quad \text{for } h \geq w$$

$$C_L = \frac{\sqrt{\Sigma reff}}{CZo} \quad \text{Where } C = 3 \times 10^{10} \text{ cm/sec}$$

$$L = C_L Z_o^2$$

$$tpd = C_L Z_o$$

$$R = \frac{\rho}{tw} \quad \text{Where } \rho = 2.8\ \mu\Omega\text{-cm (ALUMINUM)}$$

$$Z_o = \frac{60}{\sqrt{0.495\ (9.7) + 0.67}} \ln \frac{4\ (0.025)}{0.67\ (0.8\ (0.01) + 0.0008)}$$

$$Z_o = \underline{73.6\ \Omega}$$

$$\Sigma_{reff} = \frac{9.7 + 1}{2} + \frac{\Sigma r - 1}{2} \frac{1}{\sqrt{1 + \frac{10\ (0.025)}{0.01}}} = 6.2$$

$$C_L = \frac{\sqrt{6.2}}{3 \times 10^{10} \times 73.6} = \underline{1.13\ pf/cm}$$

$$L = 1.13 \times 10^{-12}\ (73.6)^2 = \underline{6.12\ nh/cm}$$

$$t_d = 1.13 \times 10^{-12}\ (73.6) = \underline{0.08\ ns/cm}$$

$$R = \frac{2.8 \times 10^{-6}}{2 \times 10^{-3}\ (2.54 \times 10^{-2})} = \underline{0.055\ \Omega/cm}$$

Figure 2-4 - Microstrip Calculations

```
          F ICONN CKT

    ICONN       CKT          91/10/28.      11.02.07.
  ** ICONN CKT **
E1  1  0  DC 0. 1R PULSE(0.,1.,.1NS,.1NS,.1NS,2.0S,4.NS)
RS  1  2  50.
R1  2  3  .05
L1  3  4  6.12N
C1  4  0  1.13F
R2  4  5  .05
L2  5  6  6.12N
C2  6  0  1.13F
R3  6  7  .05
L3  7  8  6.12N
C3  8  0  1.13F
R4  8  9  .05
L4  9  10  6.12N
C4  10  0  1.13F
RL  10  0  10.E

.END     * A ICONN TRAN
CONTROLS * SWEEP T FROM 0.NS TO 1.2NS BY .02NS
CONTROLS * PLOT 2 10*

ANALYSIS OF CIRCUIT ICONN UNDER ANALYSIS MODE TRAN

2 ITERATIONS WERE REQUIRED FOR THE FIRST POINT.
41 POINT CALCULATIONS PERFORMED IN ALL
MAXIMUM ITERATIONS 2 AT TIME 1.99999999999996E-11
MINIMUM ITERATIONS 2 AT TIME 1.99999999999996E-11


PLEASE ADJUST PAPER FOR PRINTOUT.  THEN PRESS CARRIAGE RETURN.
```

Figure 2-5 - Microstrip Coding (RAYCAD)

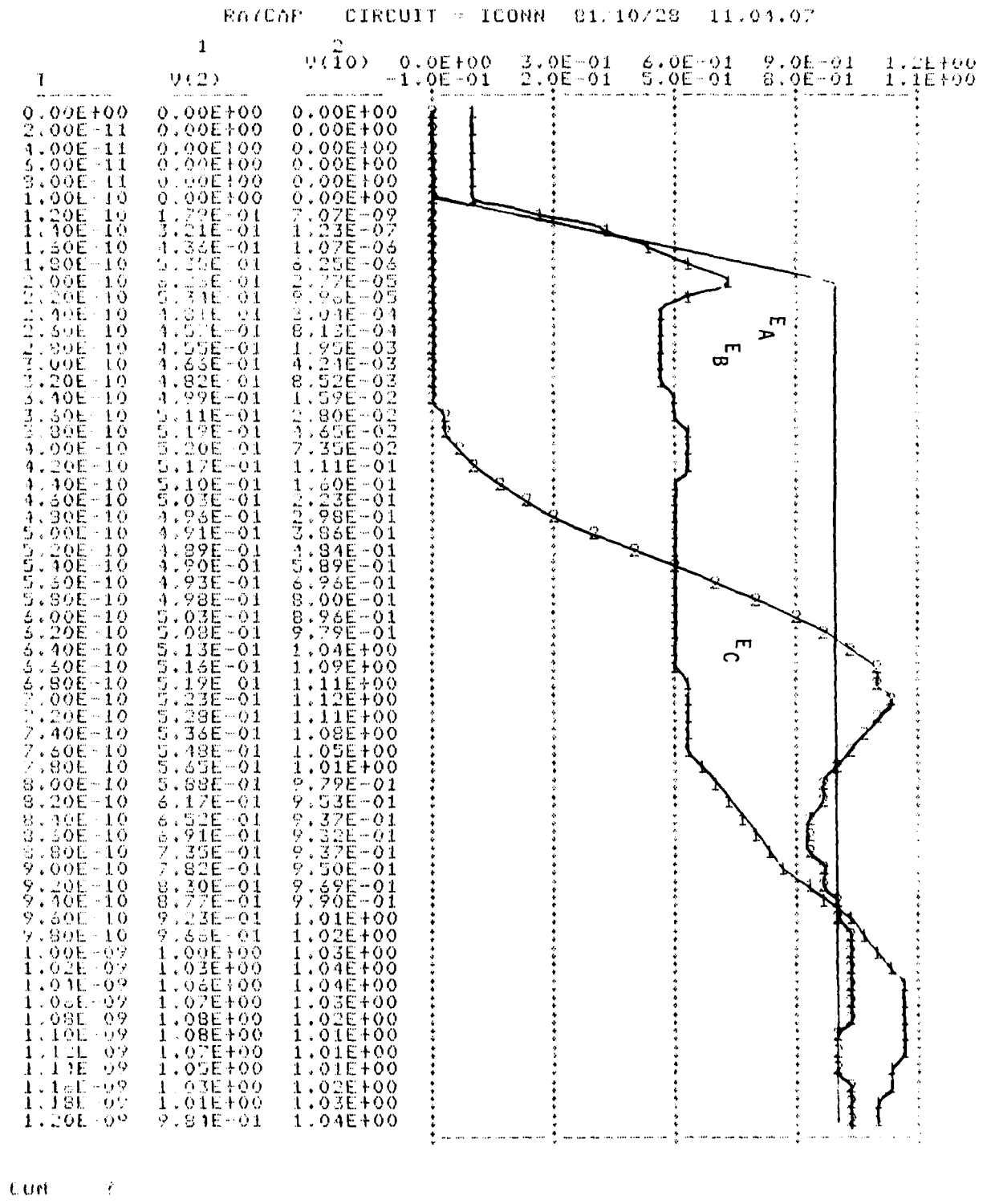


Figure 2-6 - Validation Simulation-Source Terminated Interconnect

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3. PACKAGING AND INTERCONNECT STANDARDIZATION FOR TEST CIRCUITS

The two most common state of the art hybrid circuit packaging approaches are used in this program. The first consists of a hermetically sealed "Kovar" can with metal I/O leads that protrude through glass feed-thrus. The package contains a ceramic substrate with multilayer metal interconnection patterns on its surface. Unpackaged components, such as integrated circuits, resistors, capacitors, etc. are mounted directly on the interconnection pattern. After component assembly and test, a lid is hermetically sealed to the package. This hybrid assembly is called "Chip and Wire".

The second type hybrid circuit used in this program consists of a multilayer interconnect pattern on a ceramic substrate. Ribbon input - output leads are bonded to external pads. Each active device is assembled into a leadless, hermetic chip carrier package that looks similar to a flat pack without leads. The assembled and tested chip carriers are reflow solder mounted on the interconnect pattern.

3.1 Comparison of C/W (Chip and Wire) Hybrid and Leadless Chip Carrier Packages

High density multichip hybrids that feature narrow and short interconnections are preferred to reduce propagation delay and to provide efficient thermal heat transfer from the active devices. However, in some applications multichip C/W hybrids are expensive to produce. The main cost driver is the inability to fully test the chip devices to the same extent as packaged devices. For this reason, higher rework cost is incurred. Leadless hermetic chip carriers, on the other hand, can be fully tested and burned-in and therefore result in lower rework and higher yield.

Today's leadless chip carrier packages have pads on 0.040 mil and 0.050 mil centers. These packages result in longer interconnects and increased thermal resistance in comparison to C/W hybrid packages. Of course, the increased lead length may not be detrimental in some applications.

3.2 Test Circuit Descriptions

In this program four basic interconnect configurations will be fabricated and evaluated, differing by their interconnect impedance characteristics.

Simple/Lumped	-	Interconnect only
Simple/Lumped	-	Interconnected with four different circuit families in both chip and wire and chip carrier
Microstrip	-	Interconnecting four different circuit families in chip and wire and chip carrier
Stripline	-	Interconnecting one circuit family in chip and wire and chip carrier

All test circuits for each of the selected device families are functionally equivalent and have similiar interconnect layouts to facilitate comparison and correlation between device families and packaging configurations.

Table 3-1 shows the characteristics of each of the 3 functional packaging interconnect configurations. The following paragraphs describe the packaging of each test circuit interconnect type. The simple lumped-interconnect is described in Section 5.

3.2.1 Test Pattern - Simple/Lumped with Functional Circuits

A gnd/Vcc plane (Figure 3-1) is deposited on top of the ceramic on to which successive layers of dielectric and interconnect patterns are processed. The conductors on adjacent layers are processed to be orthogonal to each other in order to achieve minimum coupling capacitance between layers. The chip and wire version of this test circuit is packaged in a conventional hybrid package.

3.2.2 Test Pattern - Microstrip With Functional Circuits

In this test pattern (Figure 3-2) the Gnd/Vcc plane is deposited on the bottom of the substrate and the conductor layers processed on the top to form a microstrip interconnect. Holes are drilled in the substrate to feed-thru interconnects from the gnd/VCC plane to pads adjacent to the active devices on the top No. 2 layer. Screening of conductor paste through the holes provides the electrical connection from the pads on the top layer to the power plane. Two versions of the microstrip test pattern have been fabricated; one with chip and wire devices in a conventional Kovar package and one with leadless chip carriers.

TABLE 3-1
TEST SUBSTRATE CHARACTERISTICS

Characteristic	Simple/Lumped		Microstrip		Stripline
	Thick Film C/W	Thick Film HCC	Thick Film C/W	Thick Film HCC	Polyimide C/W
Relative Chip Locations	X	Y	X	Y	X
Conductor Run Positions	X	Y	X	Y	X
Substrate Size	X	Y	X	Y	X
Min. Signal Conductor Width	10 mils	10 mils	10 mils	10 mils	10 mils
Min. Cond. Spacing	10 mils	10 mils	10 mils	10 mils	10 mils
Min. Via Dia. in T.F. Dielectric or Poly.	12 mils	12 mils	12 mils	12 mils	12 mils
Min. Via Dia. in Ceramic (Vcc/gnd conn's)	N/A	N/A	25 mils	25 mils	N/A
Substrate Size (inches)	1.82"x1.9"	2.8"x2.4"	1.82"x1.9"	2.8"x2.4"	1.82"x1.9"
Number of Metal Layers	4 1Gnd/Vcc 2Sig 1Bond	4	4	4	6 3Gnd/Vcc 2Sig 1Bond
Logic Test Circuitry	Same	Same	Same	Same	Same
Internal Test Point availability	Yes	Yes	Yes	Yes	Yes
External Package	Same	N/A	Same	N/A	N/A

NOTES:
"X" indicate same characteristic for C/W
"Y" indicate same characteristic for HCC

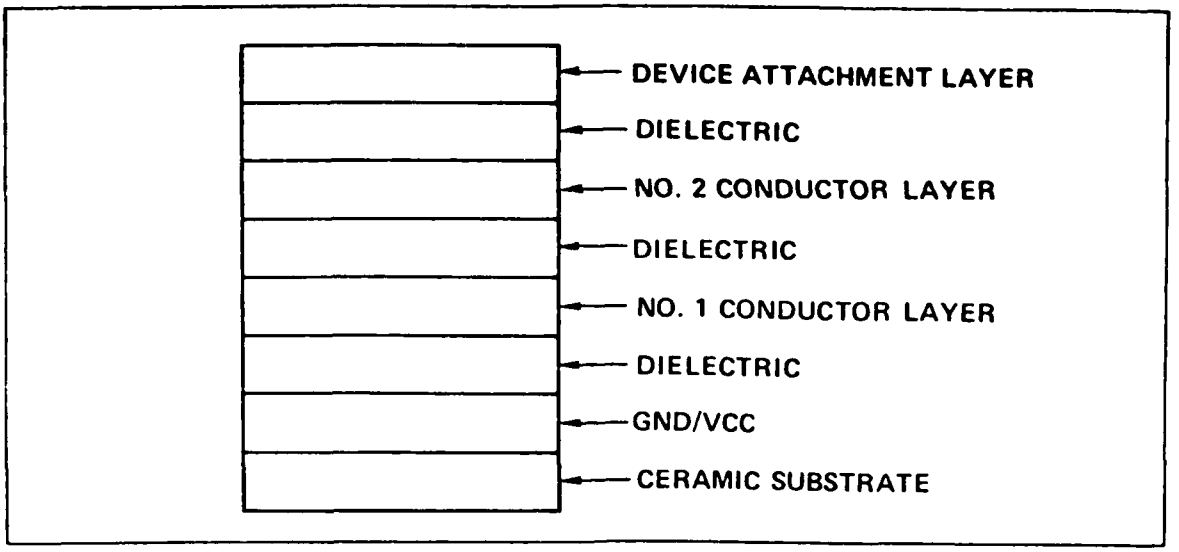


Figure 3-1 - Test Pattern - Simple/Lumped

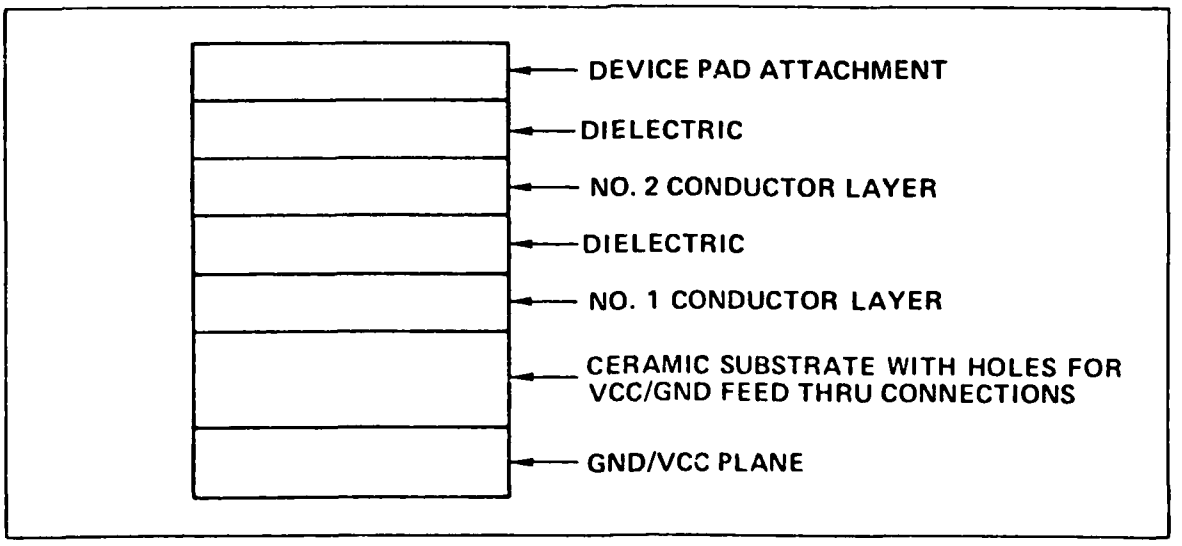


Figure 3-2 - Test Patterns - Microstrip

3.2.3 Test Pattern - Stripline with Functional Circuits

The pattern shown in Figure 3-3 also consists of 2 conductor layers, each sandwiched with a power plane on each side to form a stripline. Polyimide dielectric was chosen since it is the most expedient and low cost method to fabricate a stripline structure. Both C&W and leadless carrier versions of this test pattern will be evaluated.

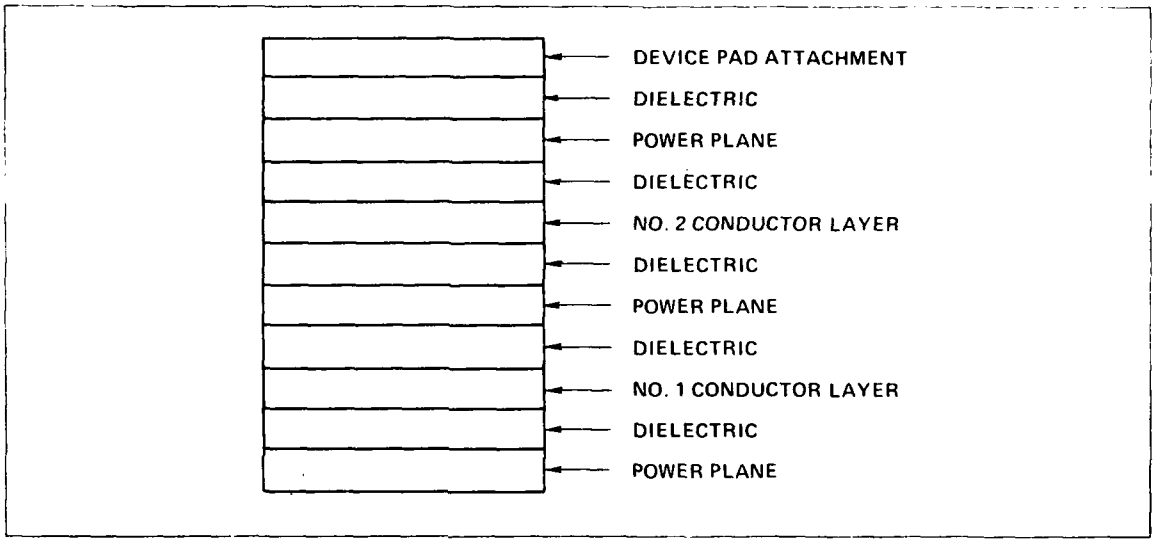


Figure 3-3 - Test Patterns - Stripline

4. LSI CHIP AND LEADLESS CARRIER THERMAL GUIDELINES STUDY

4.1 Introduction

Since thermal dissipation of the LSI devices will affect high density packaging, the objective of this study is to determine the minimum spacing possible between:

1) Hermetic chip carriers (HCCs) on alumina substrates and polyimide boards
2) Chips in hybrid packages on ceramic substrates and epoxy boards

Thermal analysis was performed on another program for 64 lead HCCs. It was conducted using the SINDA Finite Difference thermal analyzer code. These studies evaluated thermal conduction from the chip to the module substrate/board with and without a thermal checkerboard pattern (thermal conduction pads added to the HCC central location). Results indicate thermal resistances generally less than the following:

1) $5^{o}C/W$ with thermal checkerboard
2) $20^{o}C/W$ without thermal checkerboard

These values apply for chip sizes between 200 to 300 mils, which is typical for this size HCC. Power dissipations of 2 to 5 watts per chip are possible. At the larger dissipation however, a 360 mil chip must be assumed in order to limit the heat density to 39 watts/sq. in. assumed in previous studies. In this case the thermal resistance without thermal checkerboard is approximately 10^{o} C/W, while it is only $2^{o}C/W$ with the thermal pads. Therefore, the temperature difference between the chip and substrate/board is between 10^{o} C with the checkerboard pattern and 40 to 50^{o} C without it. This is summarized in Table 4-1.

The temperature differences between a typical substrate/board and the cooling air, for both direct and indirect air cooling, are discussed. Direct air cooling involves forced air convection directly over the electronic packages, while indirect air cooling utilizes forced convection through a convoluted heat sink attached to the back of the substrate/board. These results are applicable to either HCC or Hybrid type packages

TABLE 4-1

SUMMARY OF TEMPERATURE DIFFERENCES BETWEEN CHIP-TO-BOARD FOR HCCs

	With Checkerboard	Without Checkerboard
Chip Size (in.)	0.2 to 0.3	0.2 to 0.3
θ_{CB} °C/W, Thermal Resistance from Chip-to Board	5.0	20.0
T_{CB} °C at 2 W/chip	10.0	40.0
Chip Size (in.)	0.36	0.36
θ_{CB}	2.0	10.0
T_{CB} °C at 5 W/chip	10.0	50.0

within the accuracy of this study. Temperatures (substrate/board) are reported as a function of heat dissipation, density (i.e., watts/in.^{2}), and air flow rate at that level of investigation. Edge cooling with liquid is shown to be inferior except where air cooling is impossible.

LSI chips mounted in Hybrid packages are analyzed second to determine their minimum spacing. Both HCC and Hybrid package data are then combined with the previous convection data to determine the final device spacing guidelines. A limiting chip temperature of 110°C, consistent with high reliability requirements was incorporated through use of the equation;

$$T_{chip} = T_{air} + \Delta T_{air\text{-}to\text{-}board} + \Delta T_{chip\text{-}to\text{-}board}$$

The temperature difference from air-to-board through convection heat transfer is discussed and the temperature difference from chip-to-board through conduction heat transfer is discussed thereafter.

4.2 Convective Heat Transfer

Three board cooling concepts considered were:

1) Direct Cooling, Air
2) Indirect Cooling, Air
3) Edge Cooling, Liquid

Peak board temperature and pressure drop data is presented for selected board sizes and spacings. Typical system bounds were assumed to be a pressure drop of 2.0 in. of water for air cooling and, for liquid cooling, a flow rate of approximately 3.0 GPM. Fans or pumps capable of capacities greater than these are considered beyond the noise or size limitations typically imposed in military rack or cabinet applications.

4.2.1 Direct Air Cooling

The first board cooling configuration studied has air blowing directly over the devices as indicated in Figure 4-1. Air flows in the channel between card pairs, directly over the front face (device side) of one card and over the rear face of the adjacent card. Card spacings of 0.3 and 0.4 in. were evaluated. A typical ceramic board thickness of 0.060 in. was assumed to give channel gaps of 0.24 and 0.34 in., respectively.

Heat transfer coefficients were determined for fully developed turbulent flow between parallel plates using the Colburn correlation

$$N_{ST}\, N_{PR}^{2/3} = 0.023\, N_{RE}^{-0.2}$$

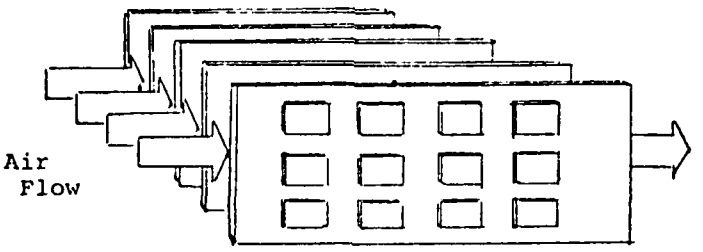
multiplied by 0.75 for noncircular channels as recommended in Reference (3). Here:

N_{ST} = Stanton Number, h/GC_p
N_{PR} = Prandtl Number, $\mu C_p/k$
N_{RE} = Reynolds Number, Gd/μ

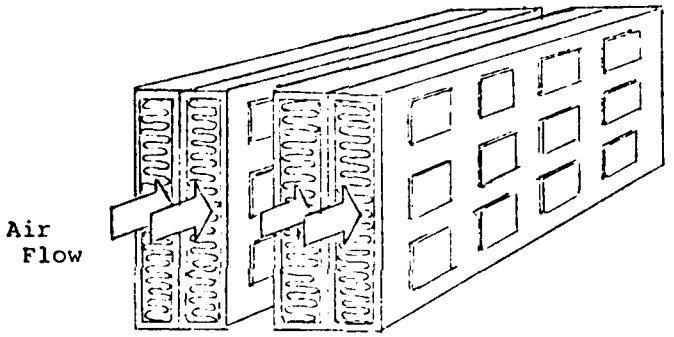
where:

h = heat transfer coefficient, BTU/hr-ft^2-^{o}F
G = mass velocity, lbm/hr-ft^2
C_p = specific heat, BTU/lbm-^{o}F
μ = absolute viscosity, lbm/hr-ft
k = thermal conductivity, BTU/hr-ft-^{o}F
d = hydraulic diameter, ft.

Direct Cooling Air



Indirect Cooling Air



Edge Cooling

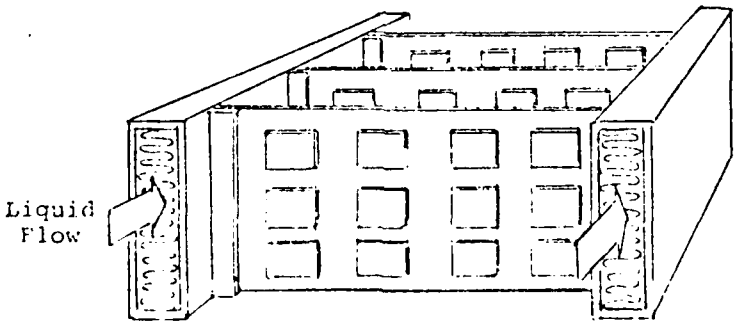


Figure 4-1 - Board Cooling Configurations

Entrance effects were then included from Reference (4) and multiplied by the fully developed values above. These values were compared with data given in Reference (5), which includes laminar and transitional flow, and agreement was found to be good. Reference (6) was subsequently used for all non-turbulent calculations.

Previous empirical studies of hybrids measuring approximately 1 in. sq. mounted on modules 6 in. long by 3 1/2 in. wide have indicated that the heat transfer can be determined with the coefficients obtained above when multiplied by the surface area of one side of the card and the factor 1.5. This factor empirically accounts for spreading of the heat in the ceramic board and also conduction through the board. This approach was considered superior to using directly heat transfer coefficients for smooth channels.

The pressure drop was estimated for zero device height by adding the friction drop for a channel of the given gap width and dynamic drop to account for entrance and exit losses. These estimates were then scaled for increased device heights using analytical as well as empirical relationships determined from previous experimental tests for comparable packaging. Heat transfer results are a weak function of device height and therefore do not significantly affect the card temperature.

The results are presented for card lengths of 6, 12 and 18 in. with a gap of 0.24 in. in Figures 4-2, 4-3 and 4-4 (0.3 in. spacing) and for a gap of 0.34 in. (0.4 in. spacing) in Figures 4-5, 4-6 and 4-7. These results are discussed together with "Indirect Air Cooling" after the next section.

4.2.2 Indirect Air Cooling

This board cooling configuration is included in Figure 4-1 for comparison with direct air cooling. Here, a finned cold plate is an integral part of each module card. Two modules are mounted back-to-back to minimize the space occupied. Air flow is "indirect" with respect to the devices, flowing only through the cold plate and not directly over the devices themselves. This method has the advantage that cooling air does not have to be as clean as it must with direct air cooling. Comparison of the space occupied by the two air cooling configurations is shown in Figure 4-8. Two types of heat exchangers both of which are available off-the-shelf were investigated for use in the cold plate. One is the KINTEX Model No. 15000, the other a Wakefield No. 4434-2 extrusion. The KINTEX exchanger has superior performance and is recommended in this application. Its core is equivalent to Kays and London No. 11.1 with performance data given in Reference (6).

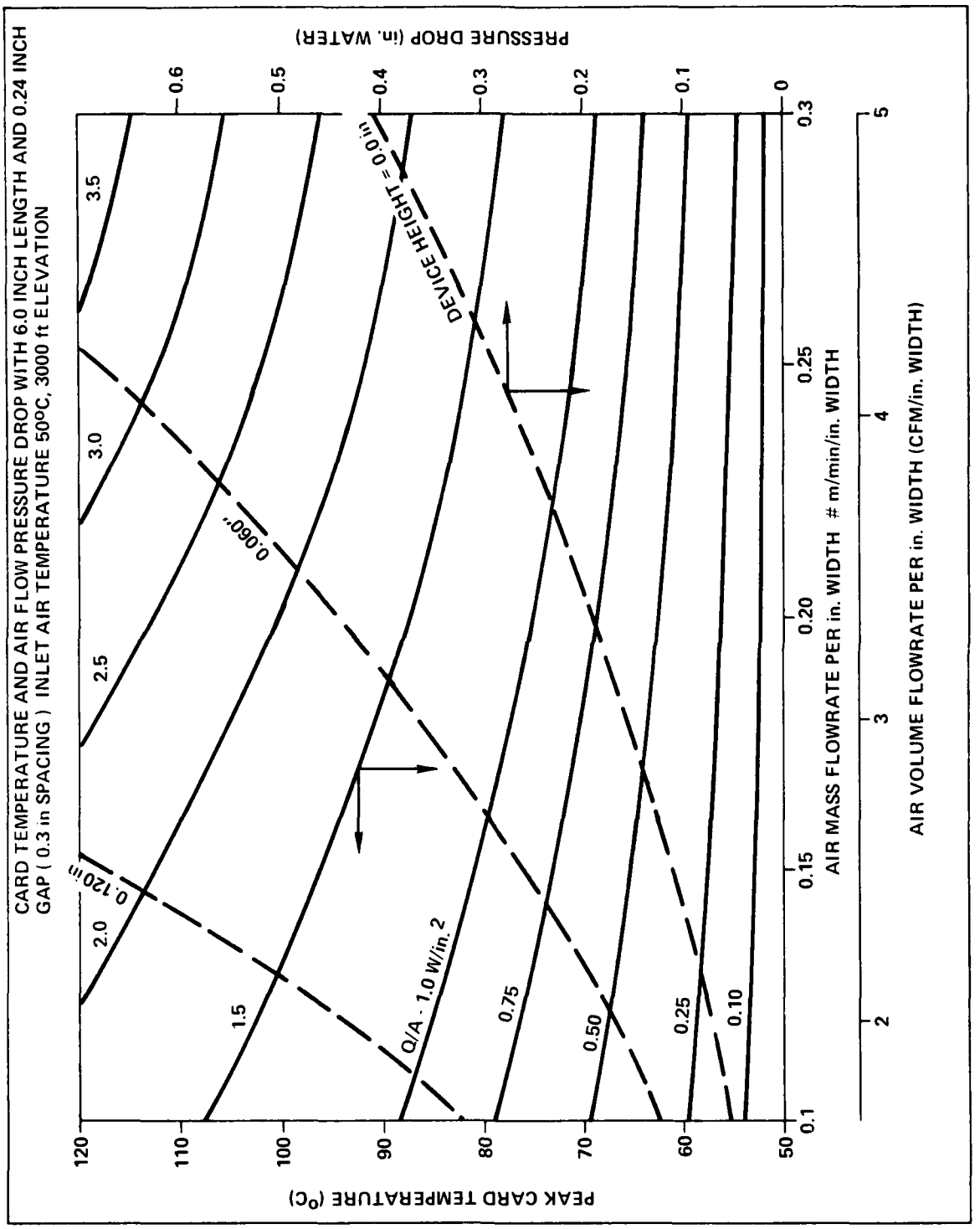


Figure 4-2 - Direct Air Cooling Data

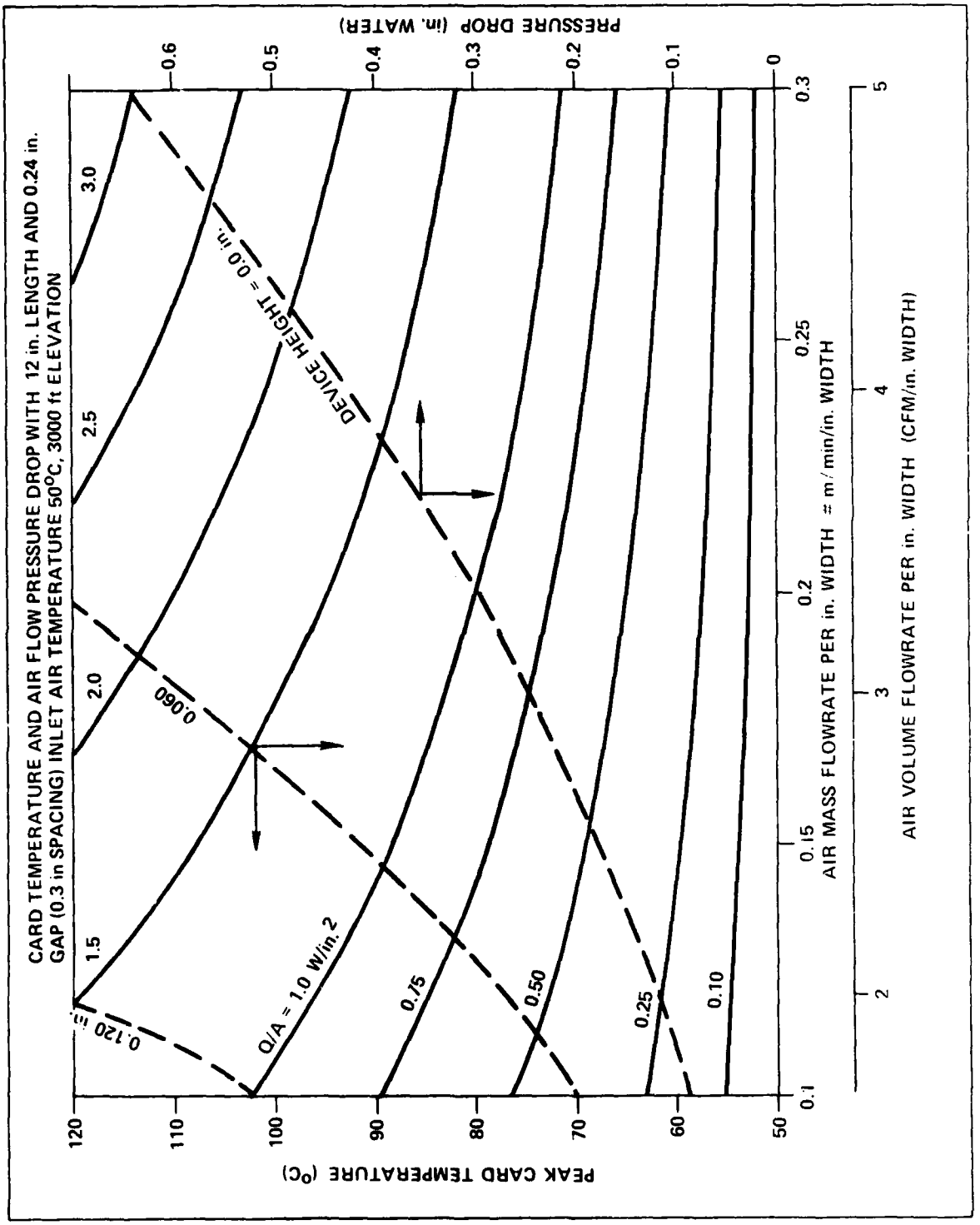


Figure 4-3 - Direct Air Cooling Data

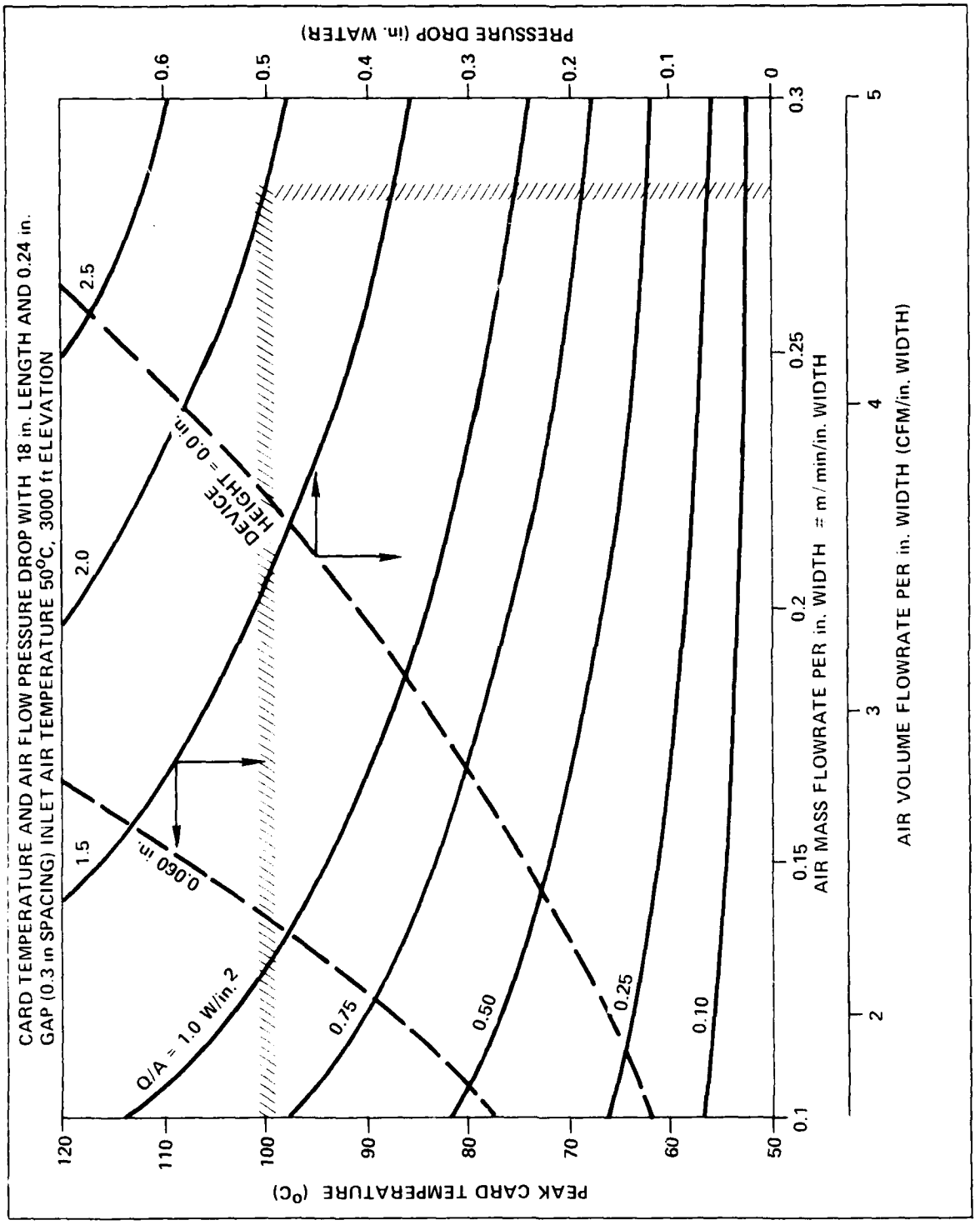


Figure 4-4 - Direct Air Cooling Data

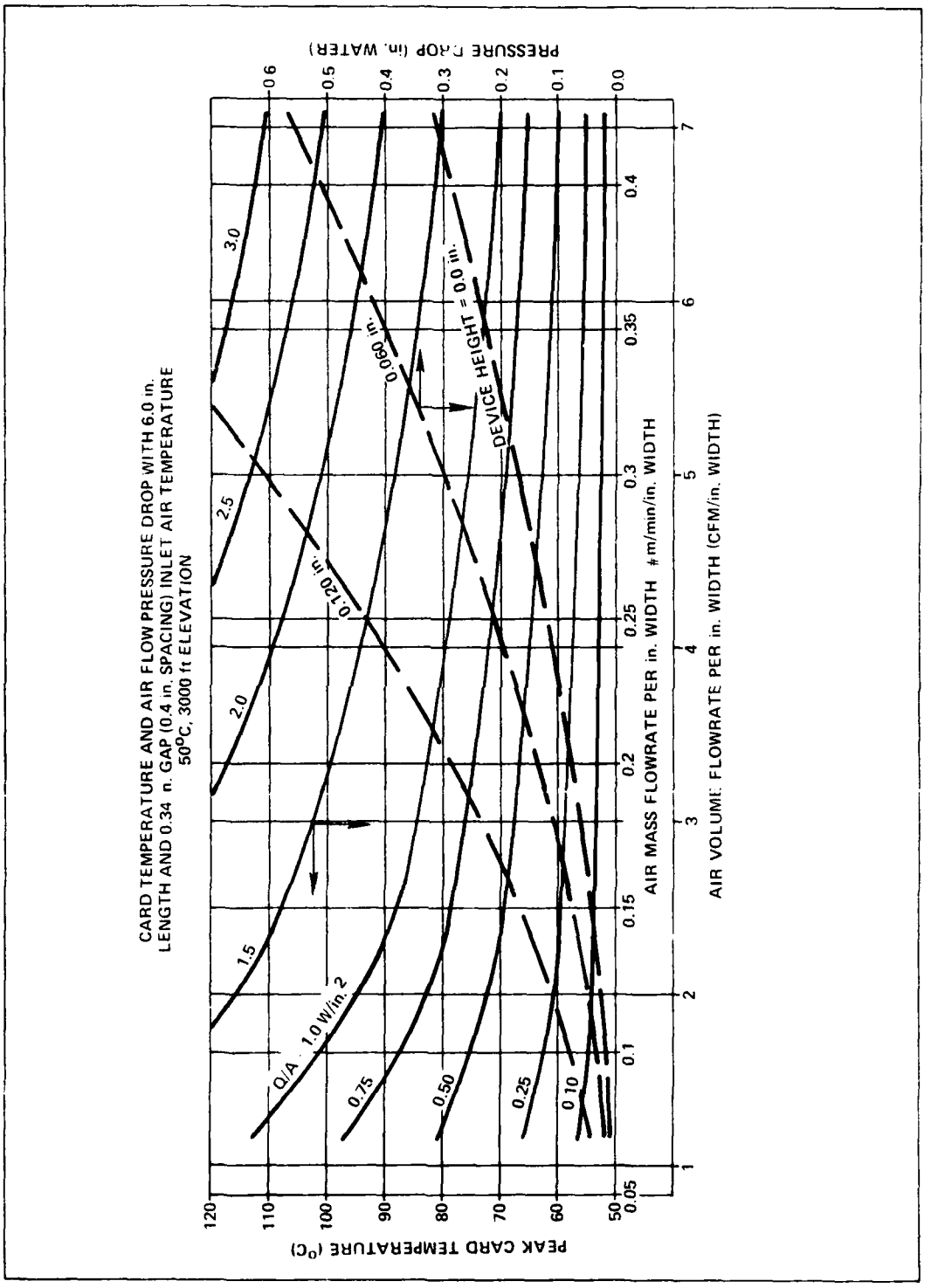


Figure 4-5 - Direct Air Cooling Data

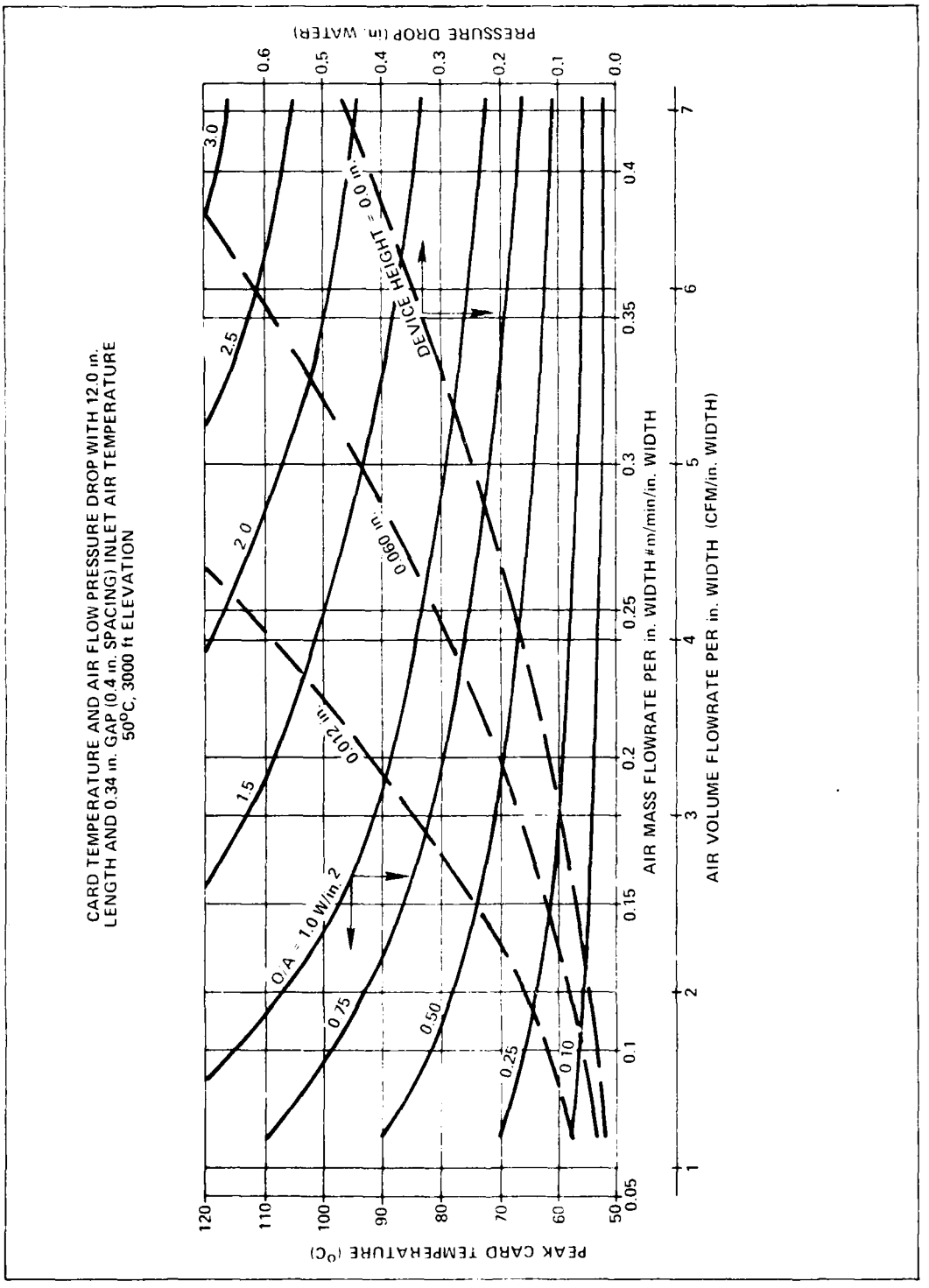


Figure 4-6 - Direct Air Cooling Data

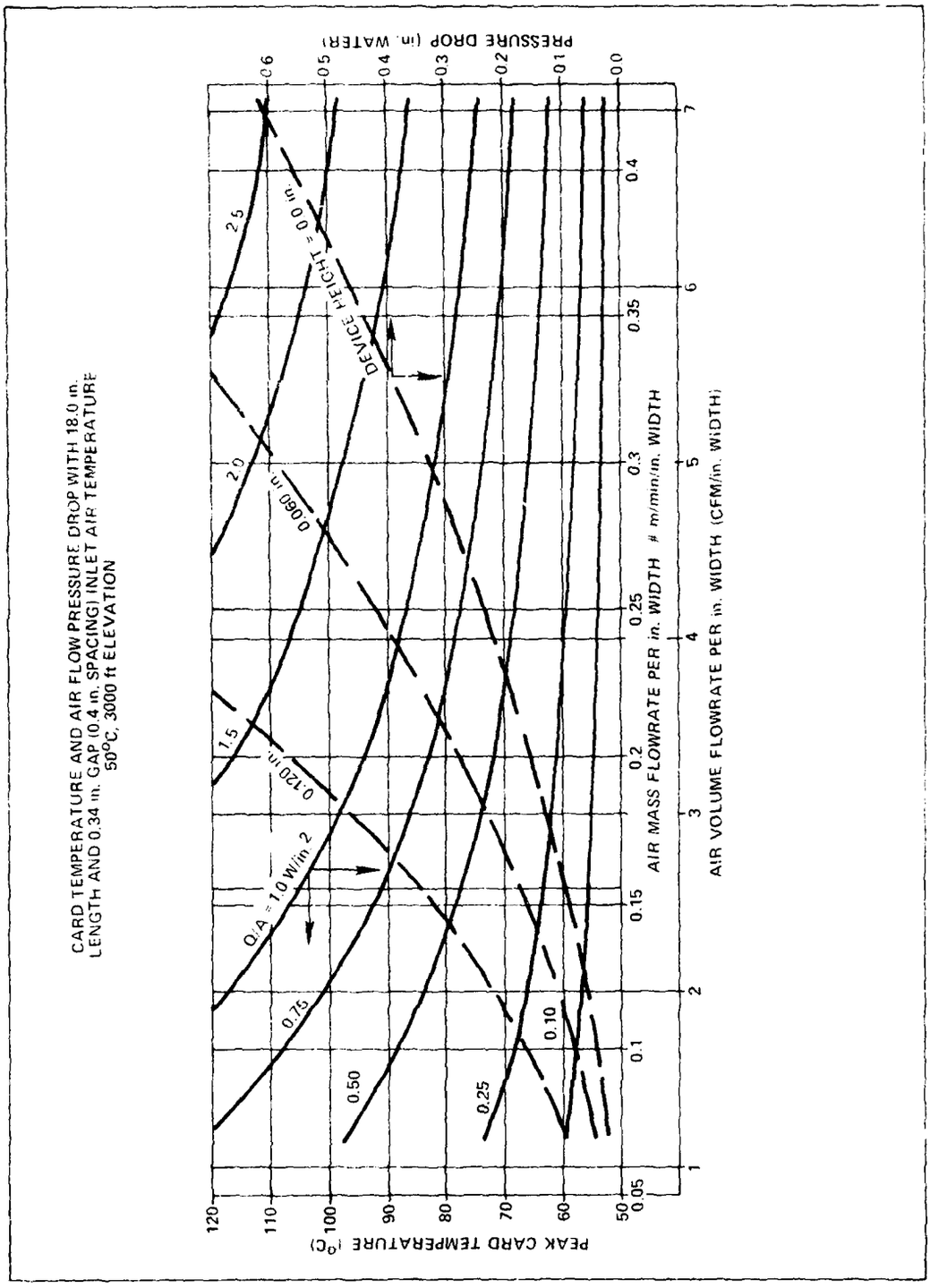


Figure 4-7 - Direct Air Cooling Data

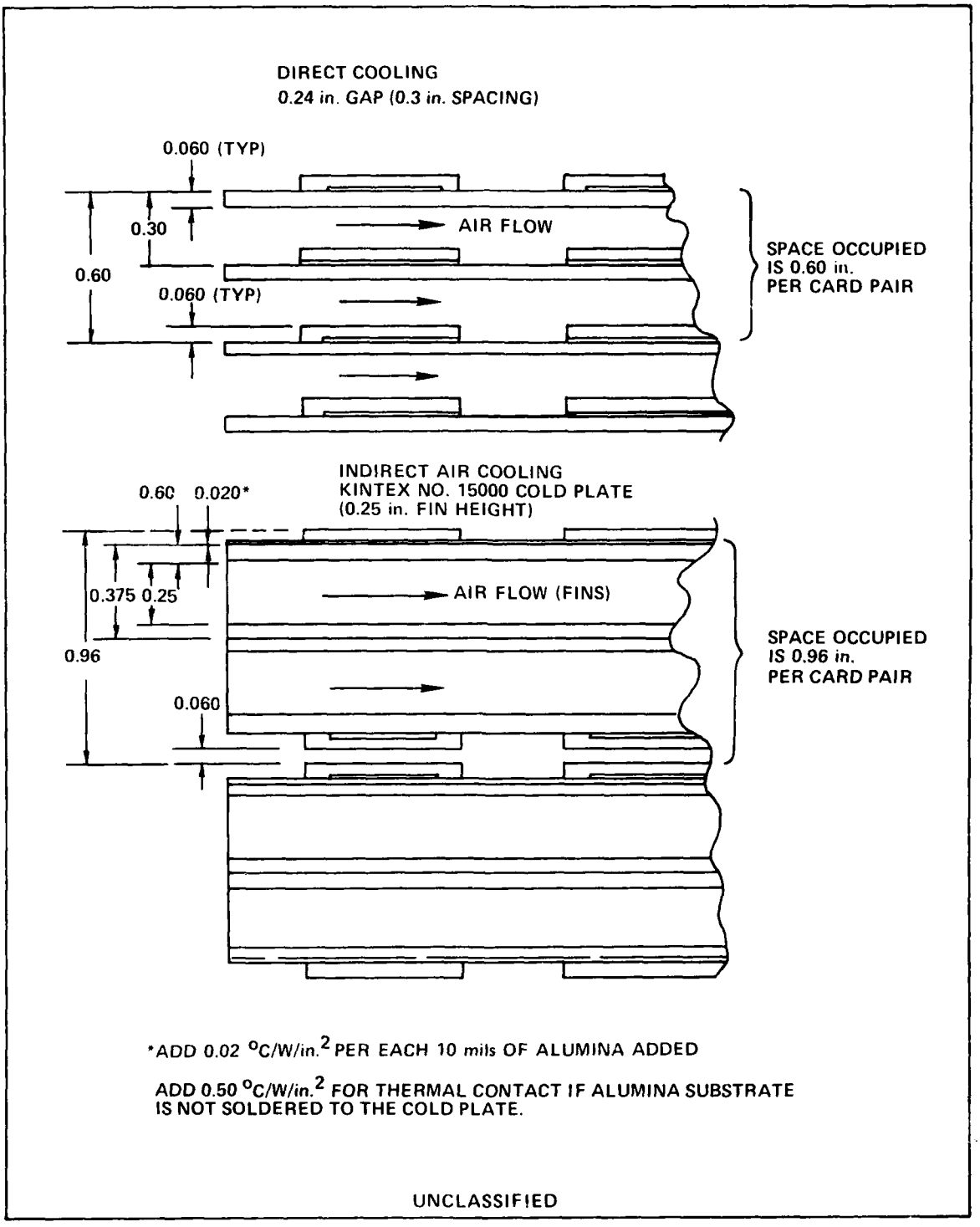


Figure 4-8 - Comparison of Configuration With Direct and Indirect Air Cooling

Here, as with the direct air configuration, a dynamic entrance and exit pressure drop was added to the friction pressure drop values. Device height is not a factor in this configuration.

Results are given for module lengths of 6 and 12 in. with a fin height of 0.25 in. in Figures 4-9 and 4-10. Results are estimated for an assumed fin height of 0.34 in. in Figure 4-11, for comparison. It is noted that this cold plate is not off-the-shelf and would require special order.

4.2.3 Air Cooling Discussion

The direct air cooling data is interpreted first. In Figure 4-2, a card temperature of 100°C is attained with a dissipation density of 2.0 watts/in.^{2} and a mass flowrate of a little more than 0.2 lbm/min/in. width. If a typical device height is assumed to be 0.060 in. this requires a pressure drop of approximately 0.45 in. water. This would infer that up to four of these cards could be arranged in a series flow path with a total drop of 2.0 in. of water. Increased air flow (hence pressure drop) would be required with multiple cards in series, however, to keep the peak card temperature at 100°C due to the *increased air temperature*. This can be seen from Figure 4-4, which approximates the results with three cards in series. This dissipation density is the typical maximum found in present day electronic packaging. If the gap between modules is increased to 0.34 in., the results of Figure 4-5, indicates that a card temperature of 100°C takes a little more than 0.3 lbm/min/in.-width and a smaller pressure drop of 0.3 in. water for a 0.060 in. device height.

The indirect air cooling data is exemplified in Figure 4-9. Here, a 6 in. long card temperature of 100°C occurs with 12 watts/in.^{2}, 0.38 lbm/min/in. width and approximately 2.0 in. of water pressure drop. Hence, the dissipation density is greatly increased, but so is the pressure drop. Increasing the fin height to 0.34 in. increases the dissipation density to 16 watts/in.^{2} while keeping the pressure drop at 2.0 in. of water (Figure 4-11).

Comparison of direct and indirect air cooling is made in Figure 4-12. The direct air cooling data from Figure 4-2 is extended to greater flowrates to allow this comparison. It can be seen here that a dissipation density of 3 watts/in.^{2} with direct air requires approximately the same flowrate and pressure drop that can handle 10 watts/in.^{2} with indirect air. It must be remembered from Figure 4-8 however, that an approximate

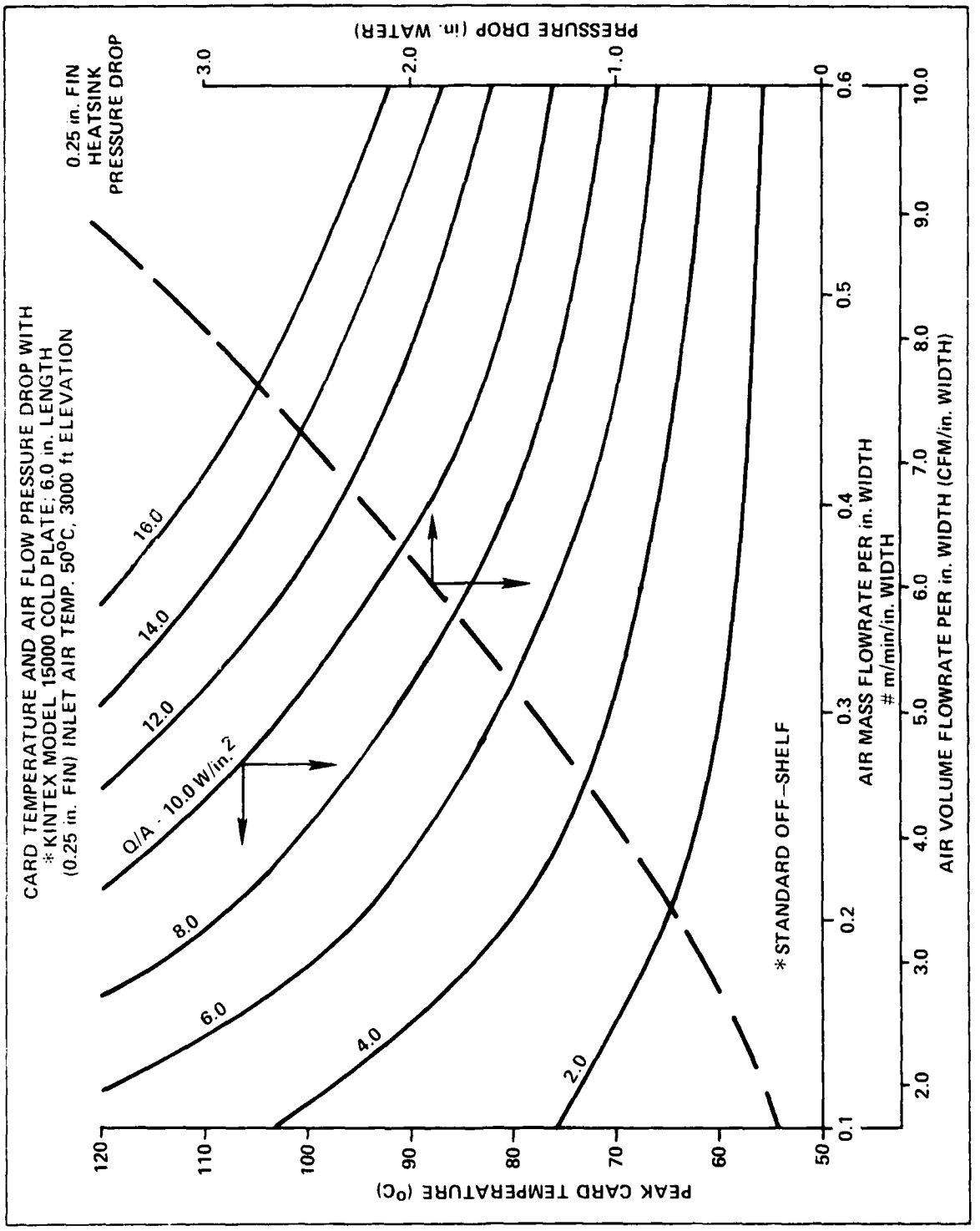


Figure 4-9 - Indirect Air Cooling Data

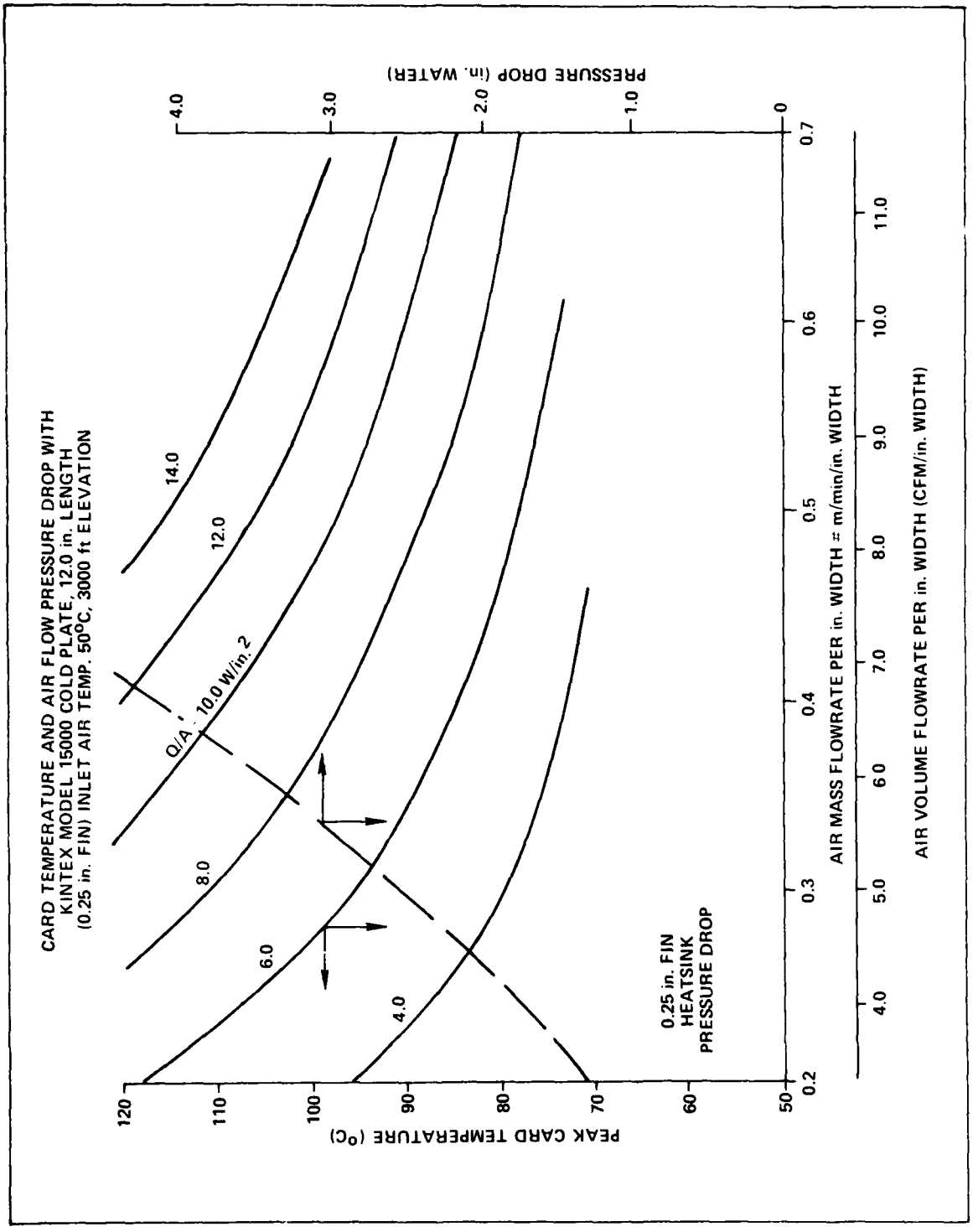


Figure 4-10 - Indirect Air Cooling Data

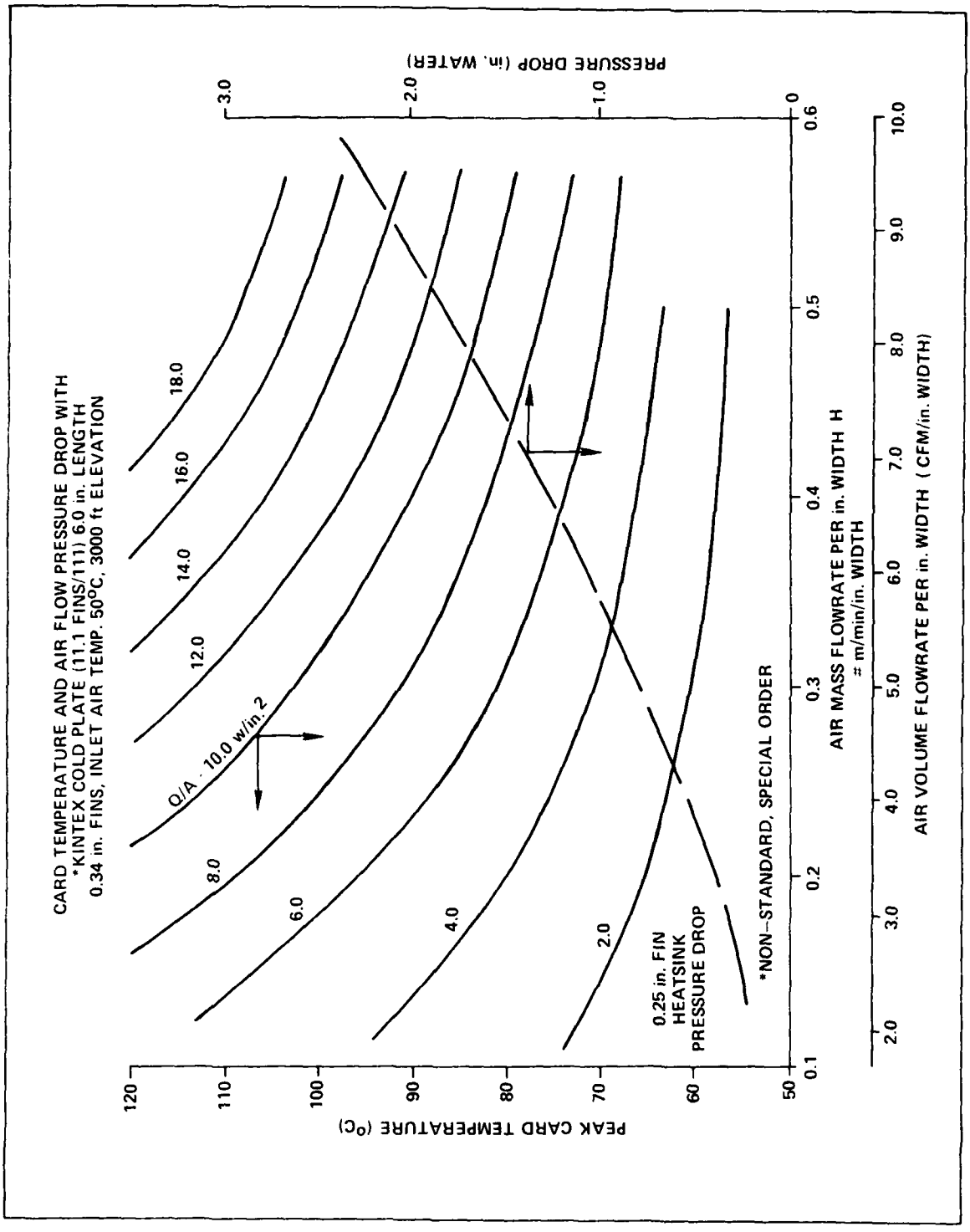


Figure 4-11 - Indirect Air Cooling Data

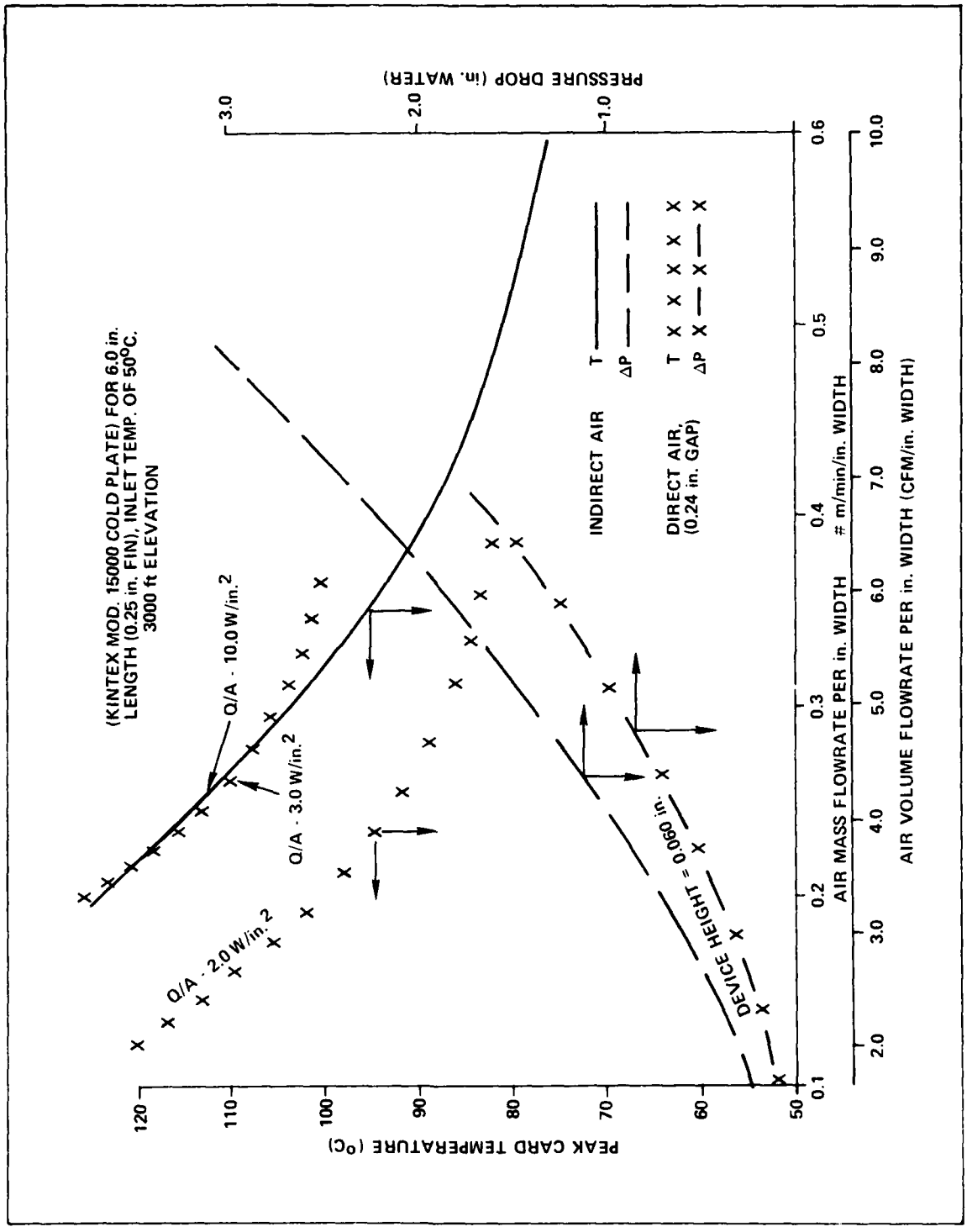


Figure 4-12 - Comparison of Dissipation Densities For Direct Air Cooling Versus Indirect Air

increase of 50 percent in packaging volume is required to utilize this indirect air configuration. Due to the increased effectiveness in heat transfer with the cold plate, greater power densities can be handled, but with shorter card lengths and a parallel arrangement of cards with regard to the air flow since a series arrangement of cards is impossible.

4.2.4 Edge Cooling, Liquid

This board cooling configuration is also depicted in Figure 4-1. The edges of the card at both ends make thermal contact with a liquid-cooled coldplate. Heat dissipated by the devices is conducted in the card to the edges in contact with the coldplate. A 1/4 in. wide thermal contact on one side only (both ends) was assumed since some sort of a spring would be required on the other side. A typical thermal contact conductance of 500 BTU/hr-ft^2-^{o}F was assumed for moderate contact pressure.

The coldplate could simply be rectangular tubing, but the spacing would have to be very small (less than 0.1 in.) to get a velocity high enough to produce the heat transfer desired (h 1000 BTU/hr-ft^2-^{o}F) with a coolant flowrate of approximately 3.0 GPM. A cold plate height of 6 in. was assumed for this calculation. A 50/50 percent by weight mixture of ethylene glycol and water was assumed as the coolant liquid. A finned cold plate such as the KINTEX 15000 was found to provide the heat transfer with a low pressure drop of only 0.05 psi per foot of length. A liquid temperature rise of only 1^{o}C would occur with 20 modules in series. An inlet coolant temperature of 50^{o}C was assumed.

A typical calculation with a 6 in. long card of 1/16 in. thick aluminum and a dissipation density of 2 watts/in.^{2} produces a total peak card temperature rise of 53^{o}C above the inlet coolant temperature (Peak Card temperature of 103^{o}C). This rise breaks down as follows:

1)	Card, center to edge	33^{o}C
2)	Thermal contact	13
3)	Coolant film	6
4)	Fluid rise	1
		53^{o}C

It can be seen that the conduction and thermal contact contributions predominate.

Results are given for 1/16 in. and 1/8 in. thick aluminum cards in Figures 4-13 and 4-14 and for 0.060, 0.080 and 0.10 in. alumina cards in Figures 4-15, 4-16 and 4-17. Results can be seen to be somewhat inferior to direct air cooling.

Edge cooling does not appear to have merit, except for cases where air cooling is impossible. If liquid cooling is pursued, an integral liquid cooled cold plate with the devices mounted directly could accommodate dissipation densities of 20 to 30 watts/in.^{2}. Significantly greater design problems because of liquid leakage would result in greater cost and complexity.

4.3 Conductive Heat Transfer

4.3.1 Hybrid Chip Analysis

A more versatile approach was used to study the conductive spreading of heat. Finite Element solutions (the ADINAT code) were employed to study chips in Hybrid packages. These analyses considered the spreading of the heat dissipated in the device packages and subsequent conduction through the substrate/board material. A typical module configuration is shown in Figure 4-18.

Chip temperatures were determined for various chip center-to-center spacing for both epoxy and polyimide boards as well as alumina substrates. Results along with material layer configurations assumed are given in Figures 4-19 and 4-20.

LSI chip size was assumed to be 0.3 x 0.3 in., each chip dissipating 2.0 watts, with a minimum spacing of 0.120 between chips (minimum center to center spacing of 0.42 in.). On epoxy or polyimide boards where spreading of the heat is significantly reduced, the chip size was assumed larger at the higher dissipations in order to limit the heat dissipation density as noted in later Figures. This limiting heat density provides an upper bound beyond which generalization is unrealistic.

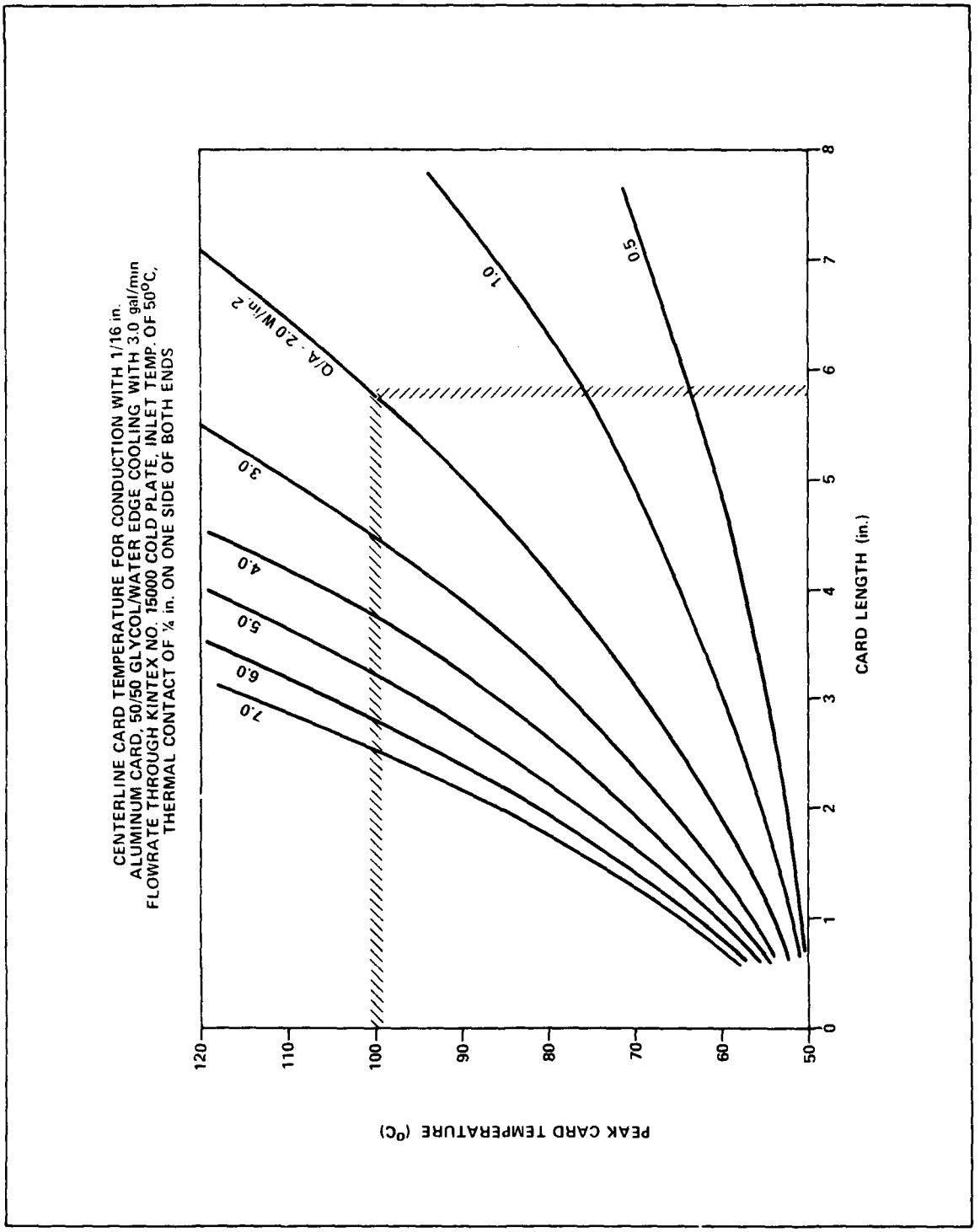


Figure 4-13 - Centerline Card Temperature For Conduction

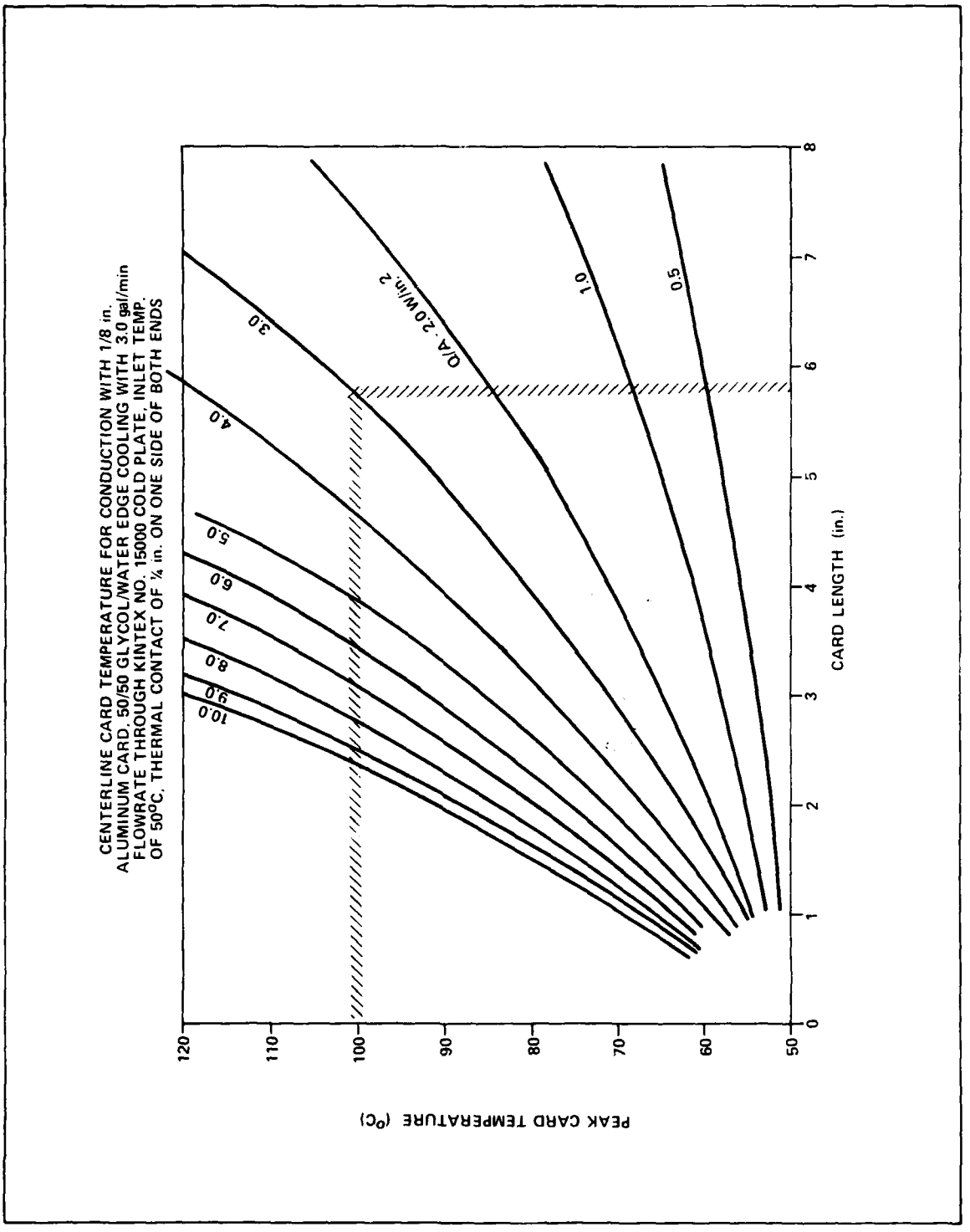


Figure 4-14 - Centerline Card Temperature For Conduction

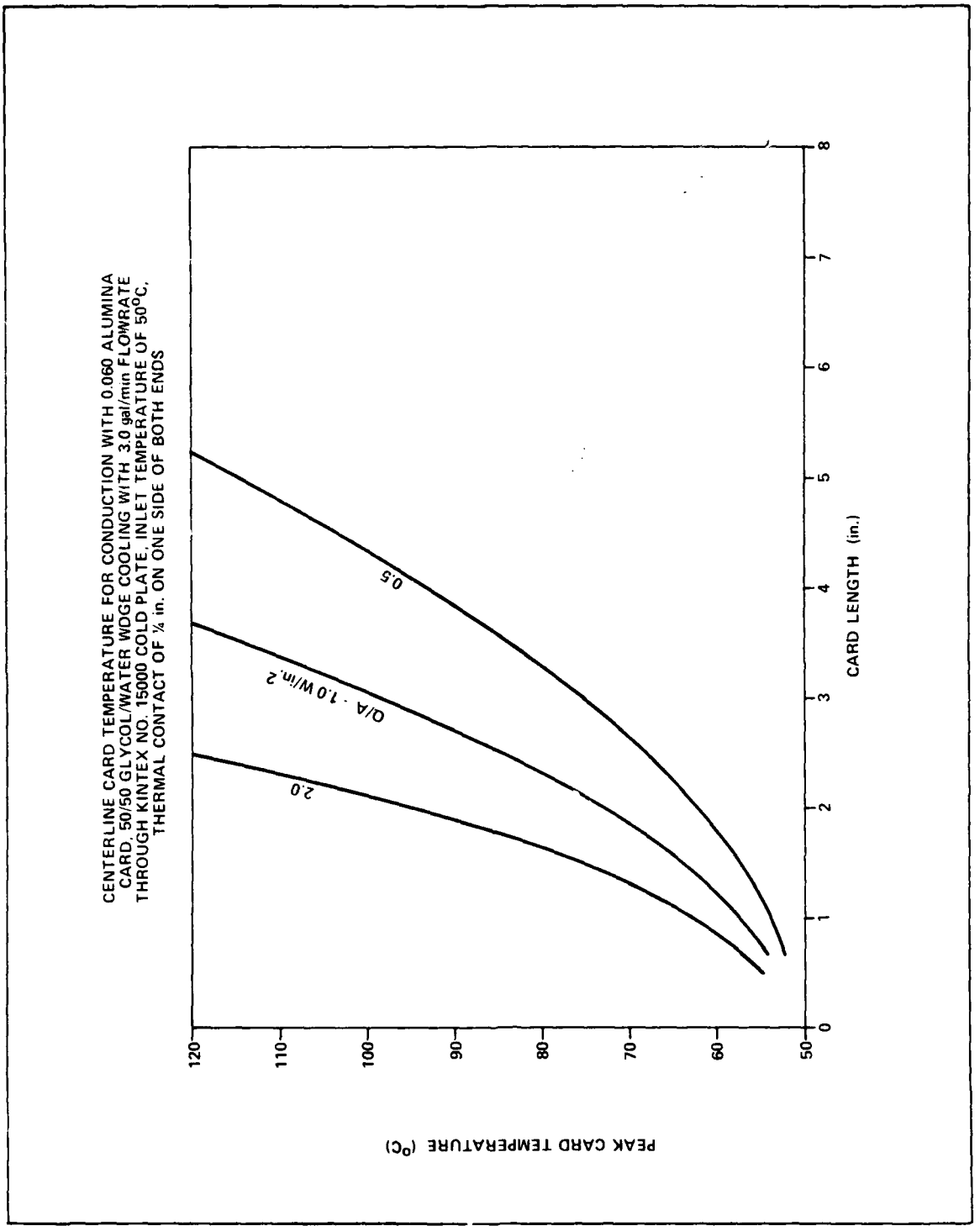


Figure 4-15 - Centerline Card Temperature For Conduction

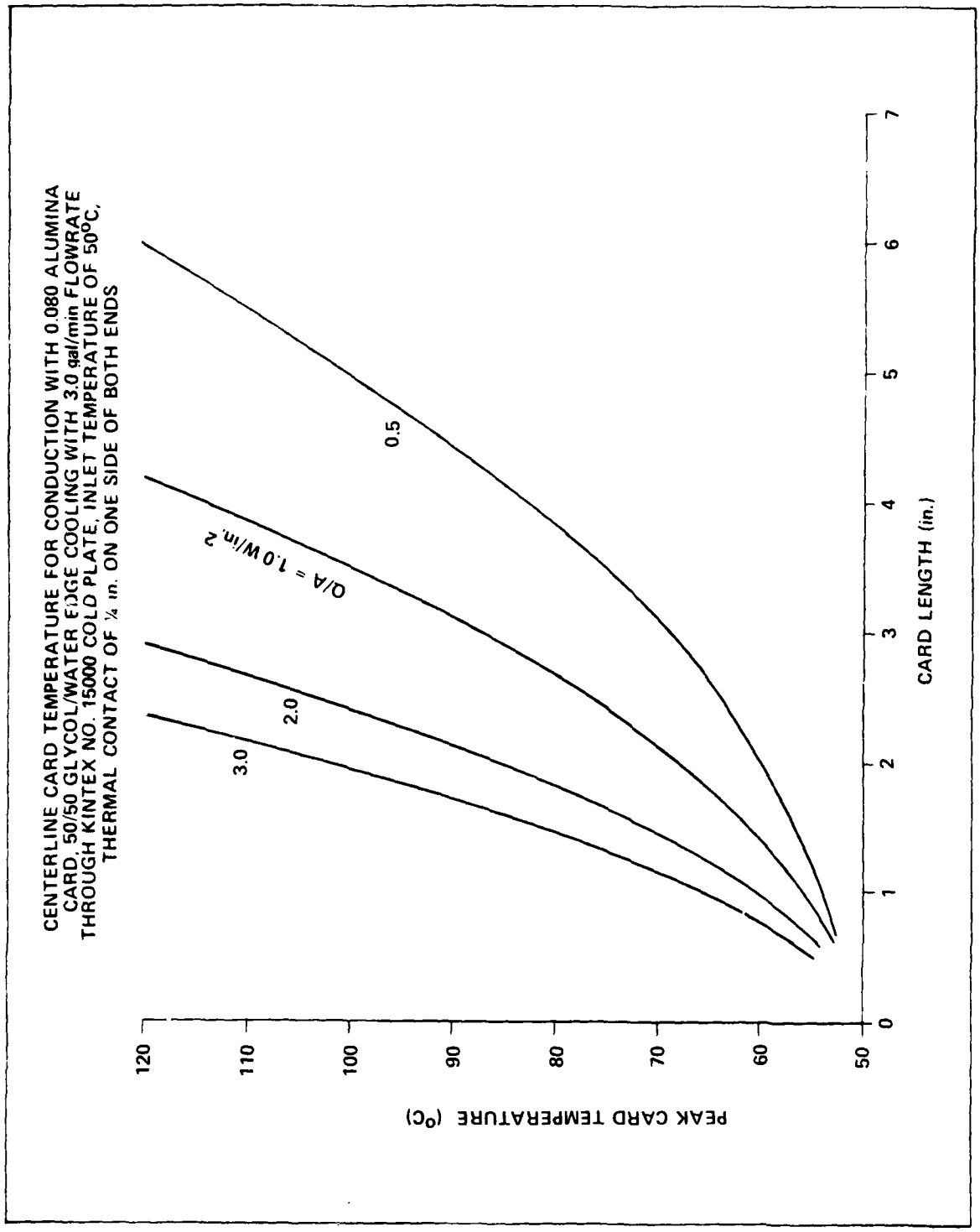


Figure 4-16 - Centerline Card Temperature For Conduction

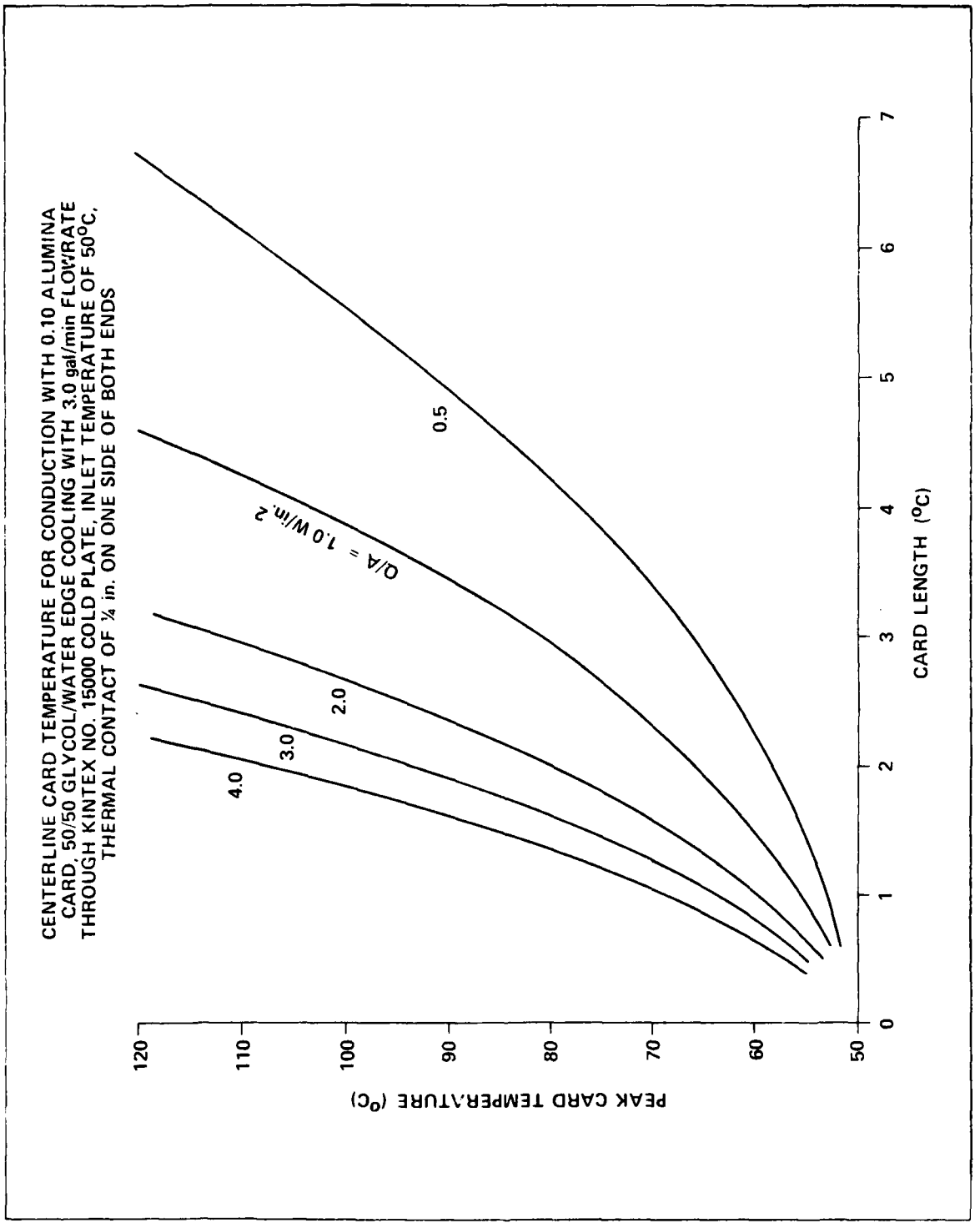


Figure 4-17 - Centerline Card Temperature For Conduction

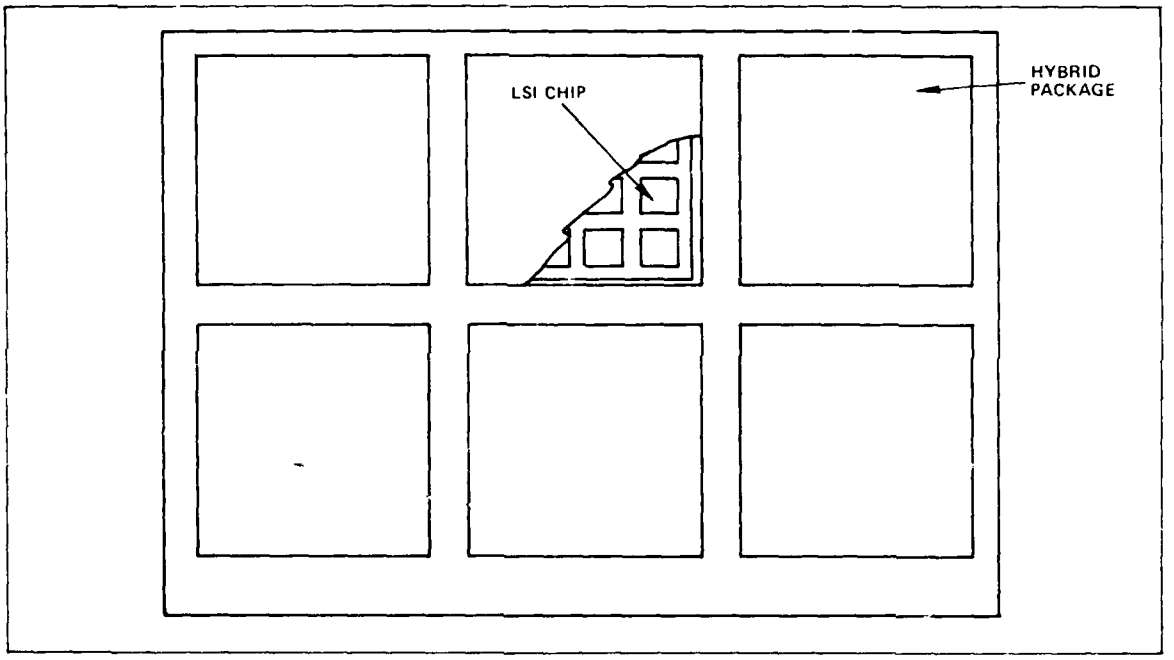


Figure 4-18 - Typical Module With Hybrid Packages

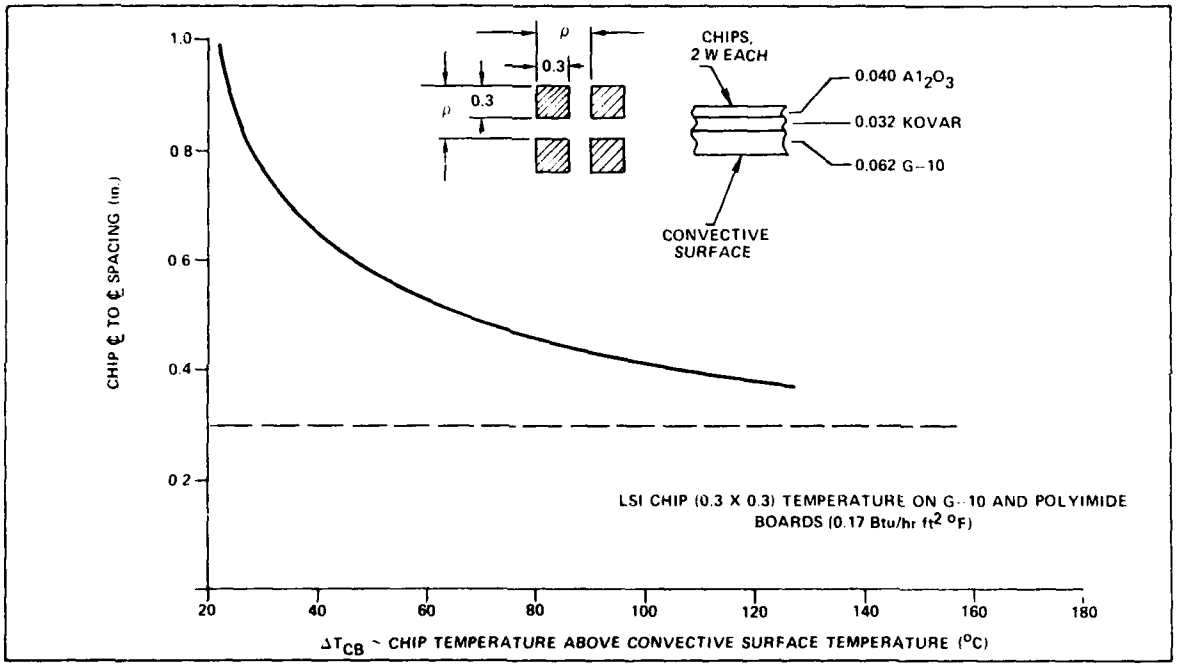


Figure 4-19 - LSI Chip (0.3 x 0.3) Temperature on G-10 and Polyimide Boards (k=0.17 BTU/in.ft°F)

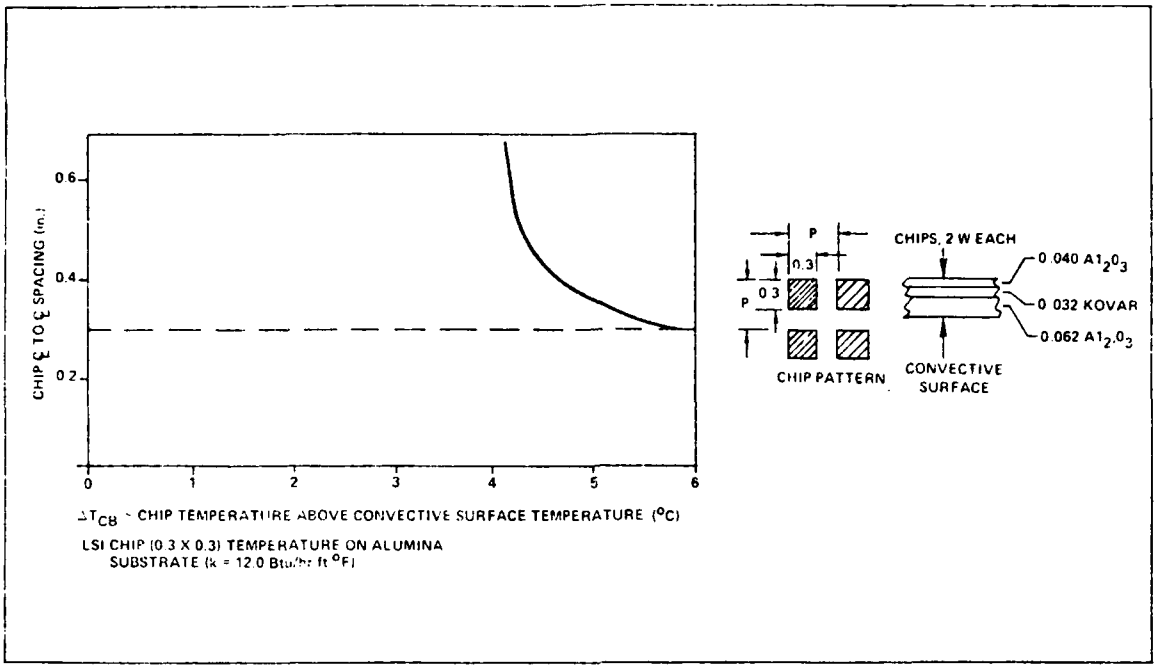


Figure 4-20 - LSI Chip (0.3 x 0.3) Temperature on Alumina Substrate (k=12.0 BTU/in.ft°F)

4.3.2 Chip Spacing Guidelines

Convective heat transfer data discussed previously for a typical 6 in. long module is summarized in Figures 4-21 and 4-22. They represent conditions of direct air cooling and indirect air cooling, respectively. As a guideline, a limiting module pressure drop of 2.0 in. water was assumed as typical, which in turn sets the mass flowrate at just under 0.4 lbm/min (6 cfm at 50°C ambient, 3000 ft elevation) in Figures 4-21 and 4-22.

It can be seen that at this limiting flowrate, the module convective surface temperature is directly related to the heat density ($W/in.^2$) at that surface. This maximum allowable heat density is generally interpreted as:

$$(Q/A)_{max} = Q_{chip}/p^2$$

where Q_{chip} is the chip dissipation and p is the chip center to center spacing (pitch, Figures 4-19 and 4-20. Likewise, the temperature difference due to conduction between the

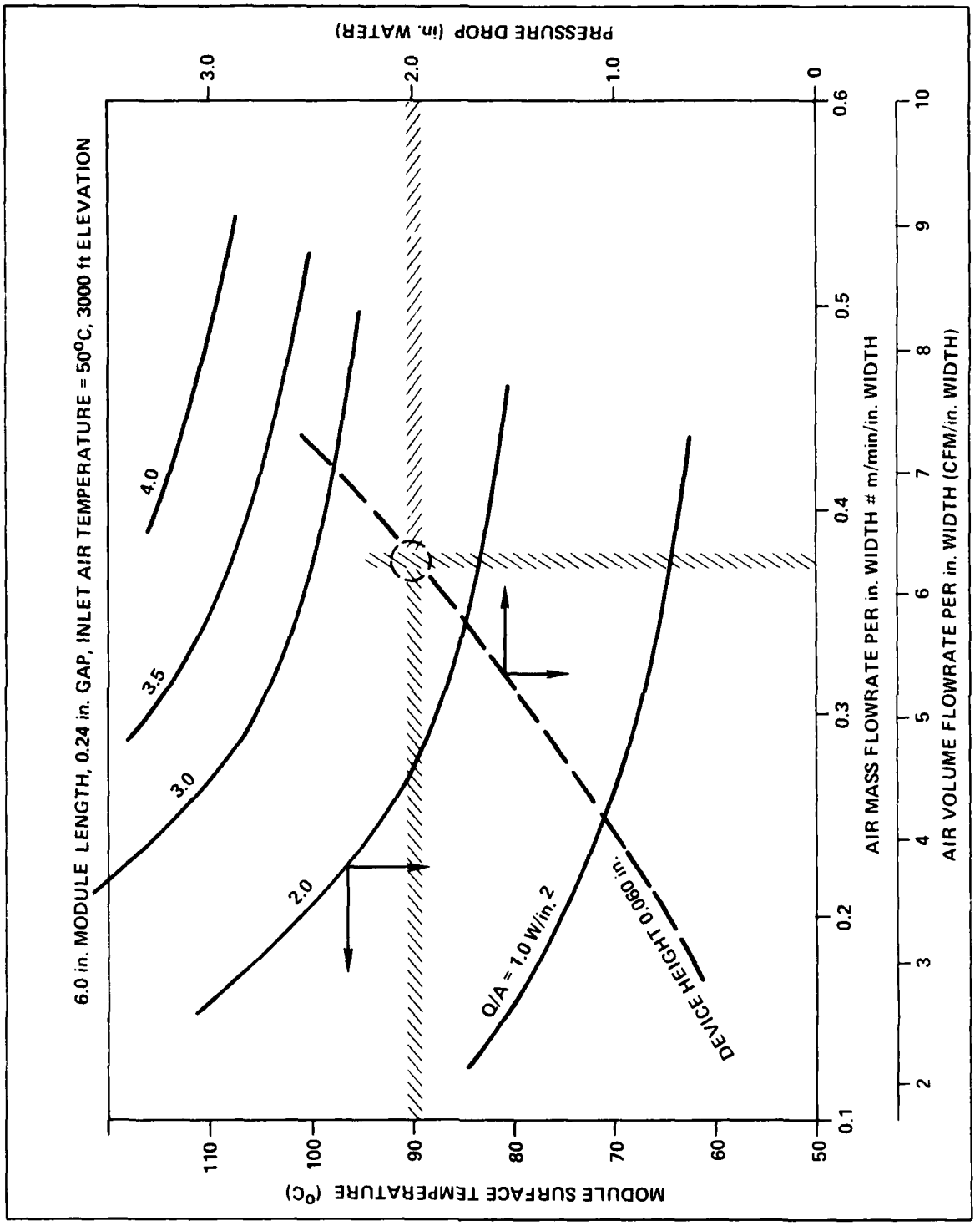


Figure 4-21 - Direct Air Cooling Data

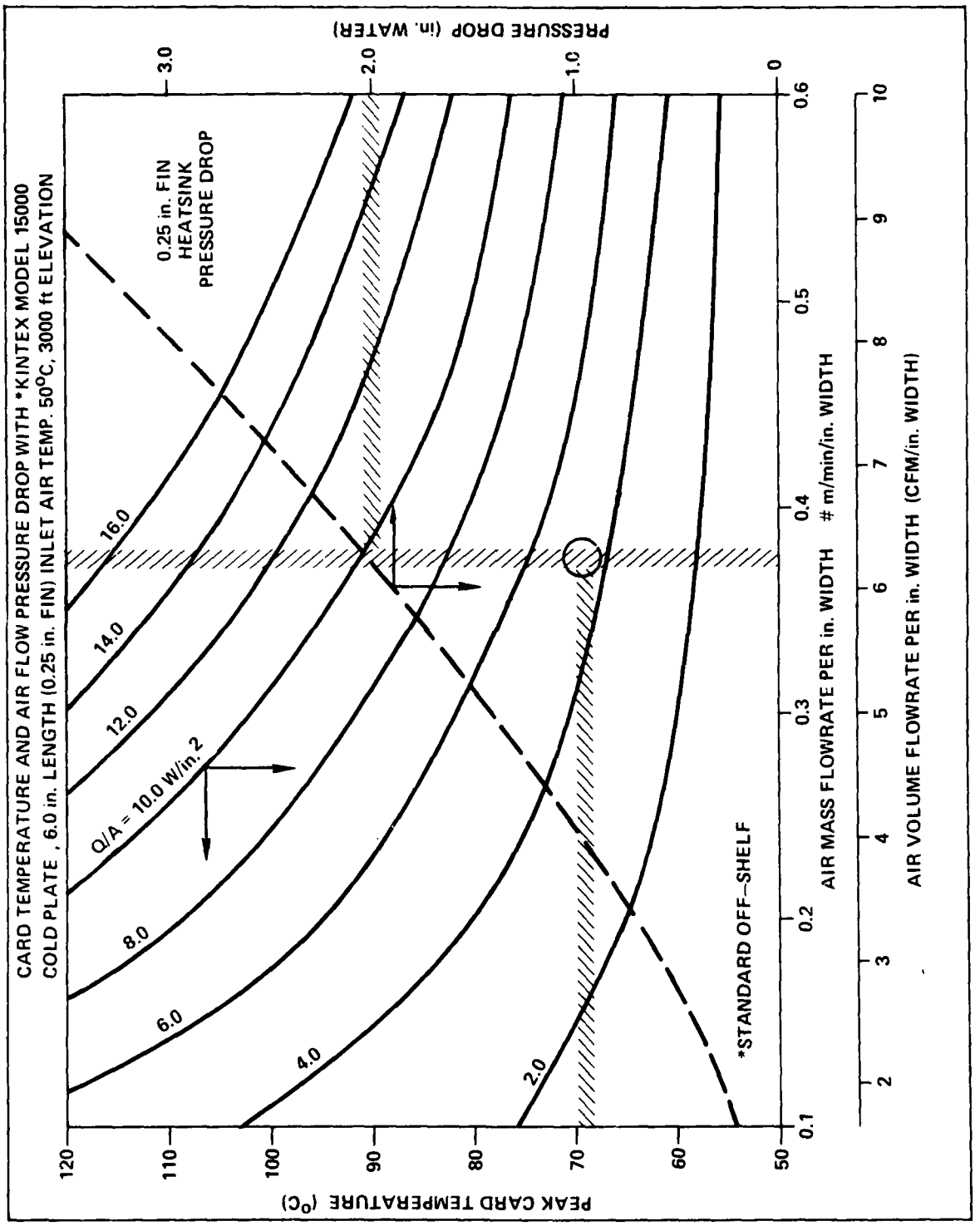


Figure 4-22 - Indirect Air Cooling Data

chip and convective surface is also related to the chip center-to-center spacing as previously described. Combining the two relations (convection and conduction) and assuming a chip temperature of 110°C, the chip spacing was determined iteratively as detailed in Table 4-2. This procedure is approximate in nature but with conservative assumptions throughout. A 25 percent safety factor was incorporated with epoxy boards when cooled by direct air to allow for some uncertainties in the lateral spreading of the heat.

The resulting device spacing guidelines for chips in HCCs are given in Figures 4-23, 4-24, and 4-25. In the case of HCCs, the spacing is for HCC packages, not chips. The curves represent the boundaries between direct air cooling, indirect air cooling and further improved cooling such as liquid cooling. Operating points itemized indicate the cooling regimes required for the 64 lead HCCs studied (0.72 in. x 0.72 in. with 0.10 in. spacing) with center-to-center spacing of 0.82 in. and chip dissipations of 2 and 5 watts each. Operating at 5 watts with air cooling at this spacing can only be accomplished with HCCs, if the thermal checkerboard pattern is utilized and the packages are mounted on alumina substrates. Operation without the checkerboard pattern would require a spacing greater than 1.0 in. for indirect air cooling. Operation without the checkerboard pattern on polyimide boards is not recommended.

The center-to-center spacing guidelines between chips in Hybrid Packages are given in Figures 4-26 and 4-27. Operation at 2 watts chip dissipation with a center to center spacing of 0.42 in. is seen to be borderline at best with indirect air cooling and an alumina board/substrate. Operation at 2 watts with a G-10 board would require chip center-to-center spacing greater than 0.70 in. if indirect air cooling is desired.

A final note is that the curves in Figures 4-23 through 4-27 could all be shifted downwards to give smaller spacings if the temperature difference between the chips and the board/substrate convective surface can be reduced. Engineering of individual board designs to provide improved conductive paths are possible.

TABLE 4-2

SAMPLE CALCULATION FOR CHIP AND WIRE DEVICE ON G-10 BOARD

Direct Air Cooling

Let Q_{chip} = 1.0 W (half of that used in Figure 4-19)

Thru iteration of the following procedure determine p = 0.65 in.. From Figure 4-19

$$\Delta T_{chip\text{-}to\text{-}board} = 1/2\ (40) = 20^{o}C$$

Convective surface temperature is

$$T_{board} = 110 - 20 = 90^{o}C$$

From Figure 4-21 the convective surface heat density allowable is

$$(Q/A)_{max} = 2.4\ W/in.^2$$

With a center to center spacing of 0.65 in. the heat density at the convective surface would be

$$Q/A = \frac{1.0}{(0.65)^2} = 2.4\ W/in.^2$$

confirming the spacing determined.

Assuming a 25% safety factor for lateral spreading of heat in the epoxy board.

The guideline spacing recommended is

$$0.65 \times 1.25 = 0.81\ in.$$

Indirect Air Cooling

Let Q_{chip} = 1.0 watt (half of that used in Figure 4-19)

Through iteration determine p = 0.46

From Figure 4-19

$$\Delta T_{chip\text{-}to\text{-}board} = 1/2\ (82) = 41^{o}C$$

Convective surface temperature is

$$T_{board} = 110\text{-}41 = 69^{o}C$$

TABLE 4-2 (Cont'd)

From Figure 4-22 the convective surface heat density allowable is

$$(Q/A)_{max} = 4.7 \text{ W/in.}^2$$

With a center to center spacing of 0.43 in., the heat density at the convective surface would be

$$Q/A = \frac{1.0}{(0.46)^2} = 4.7 \text{ W/in.}^2$$

confirming the spacing determined.

A safety factor is not necessary with indirect cooling due to the higher degree of certainty of the spreading of the heat. The guideline spacing recommended is therefore 0.43 in.

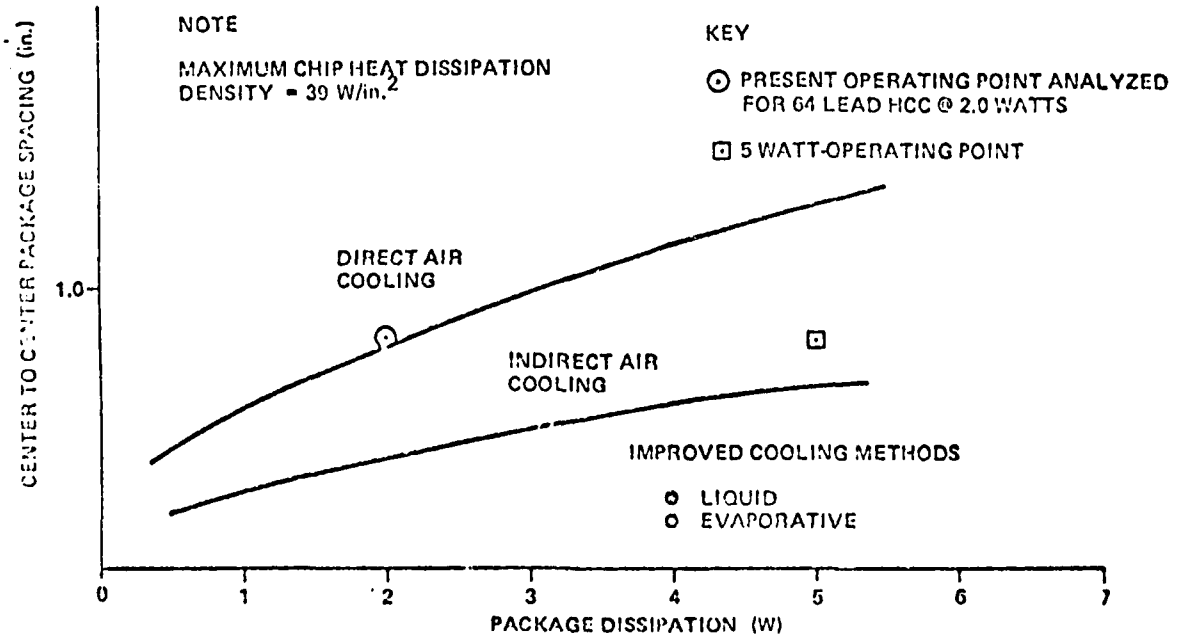


Figure 4-23 - HCC Package With Thermal Checkerboard Pattern On Alumina Substrate

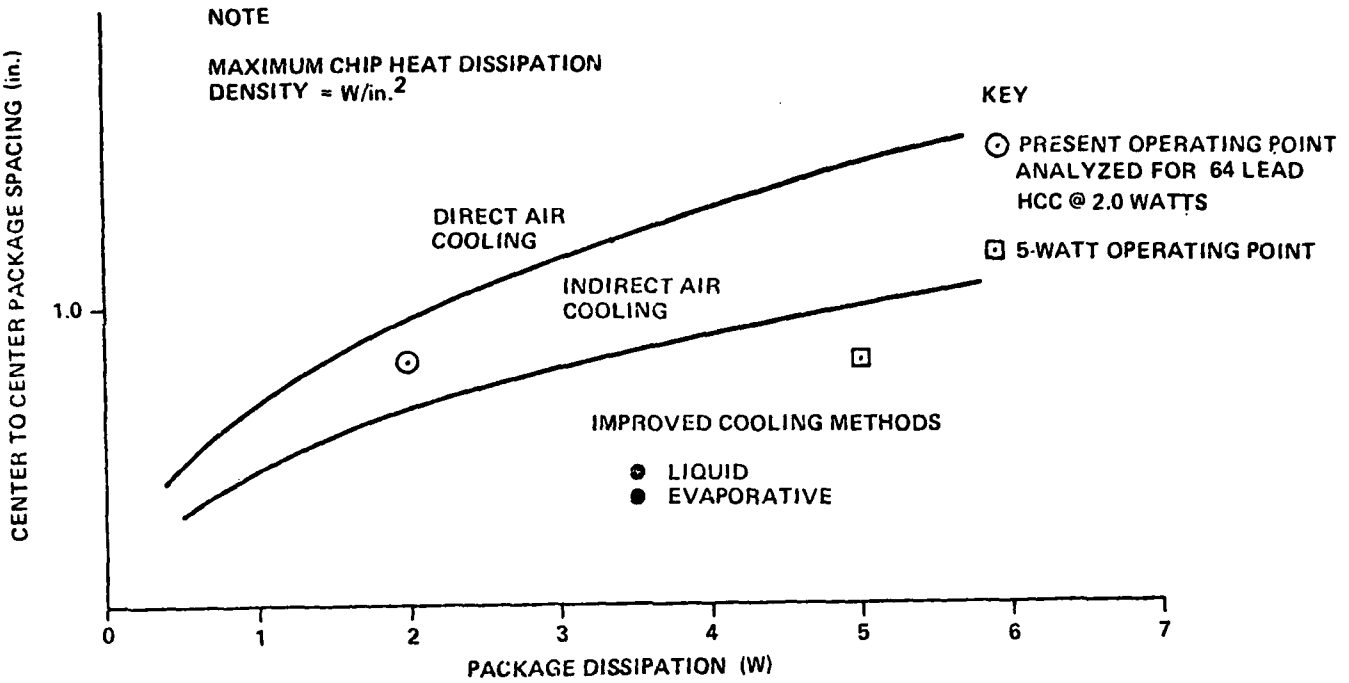


Figure 4-24 - HCC Package With Thermal Checkerboard Pattern On Polyimide Board

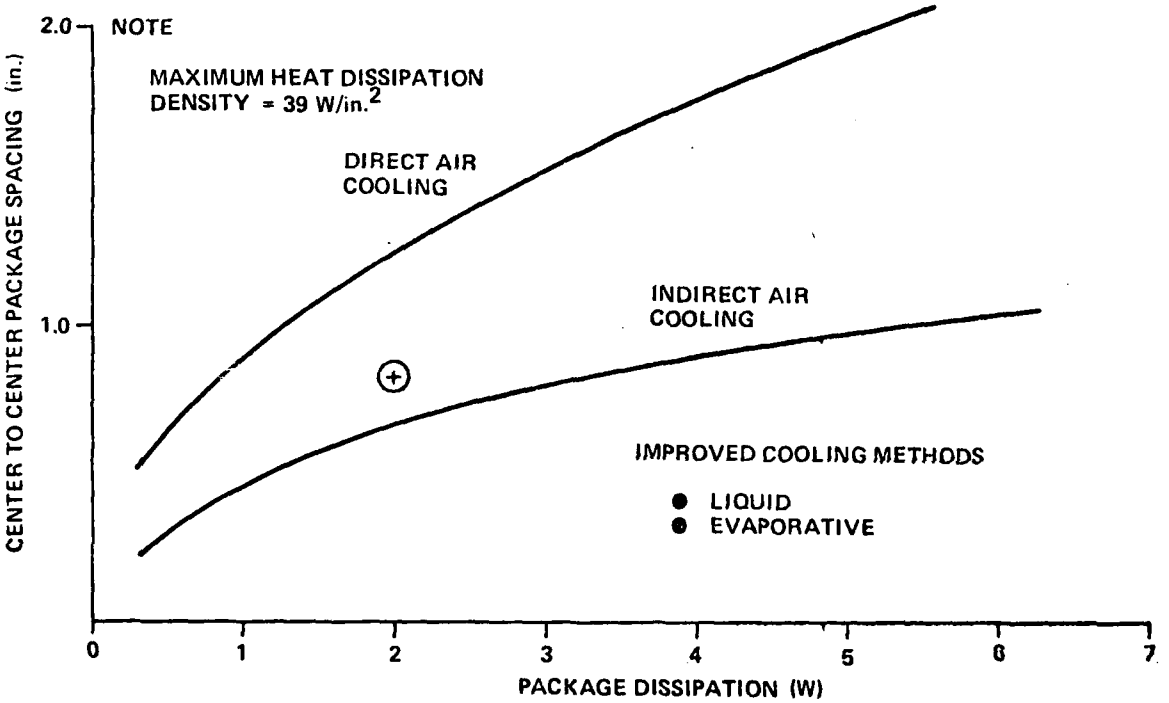


Figure 4-25 - HCC Package Without Thermal Checkerboard Pattern On Alumina Substrate

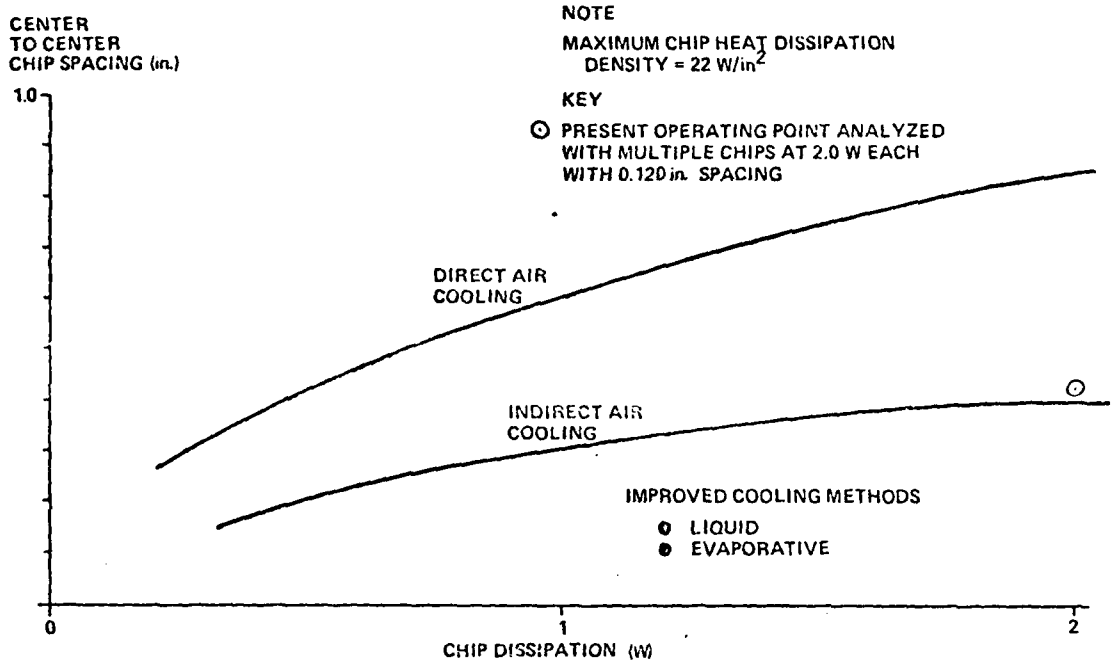


Figure 4-26 - Chip and Wire Device In Alumina Package On Alumina Board

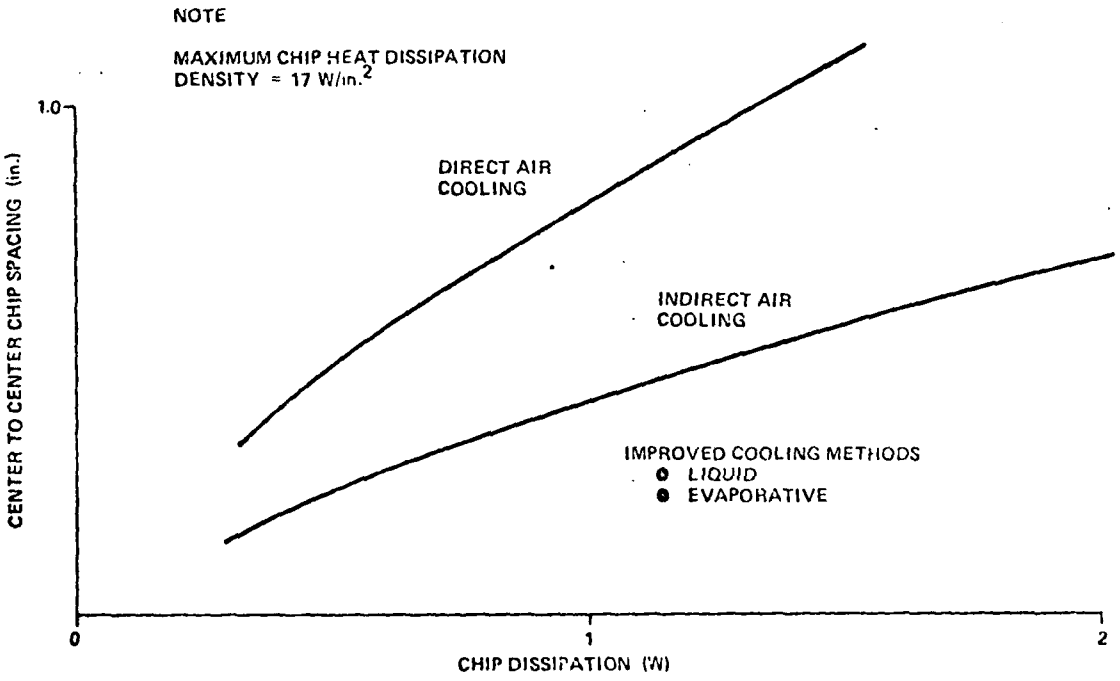


Figure 4-27 - Chip and Wire Device In Alumina Package On G-10 Board

5. INTERCONNECTION TEST SUBSTRATE

To aid in the interconnect model validation a test substrate was designed. The type construction is simple/lumped. A simple representation is shown in Figure 5-1. The test substrate is used to evaluate the all-important test equipment interfaces.

5.1 First Interconnection Layer

The first interconnect layer is shown in Figure 5-2. Each trace is identified with a number. The following details the purpose of each interconnect:

Lines 1, 2 & 3	-	Long parallel interconnects with varied spacing. Cross talk evaluation.
Lines 4, 5 & 6	-	Interconnects of various lengths.
Line 7	-	An interconnect with 90 deg bends.
Line 8	-	An interconnect with 45 deg bends.
Line 9	-	Part of a serpentine interconnect. This line is completed when the second layer is added. Evaluates a line with ten vias.
Line 10	-	Single interconnect parallel to a coplaner interconnect. Isolation evaluation.
Line 11	-	Coplaner configuration. Isolation evaluation.
Line 12	-	Part of another serpentine interconnect that is completed when a second layer is added. This has five vias.

Note, that a large square pattern is provided at the bottom to form one plate of a parallel plate capacitor. The other plate is the power plane directly underneath. It will be used to evaluate dielectric thickness.

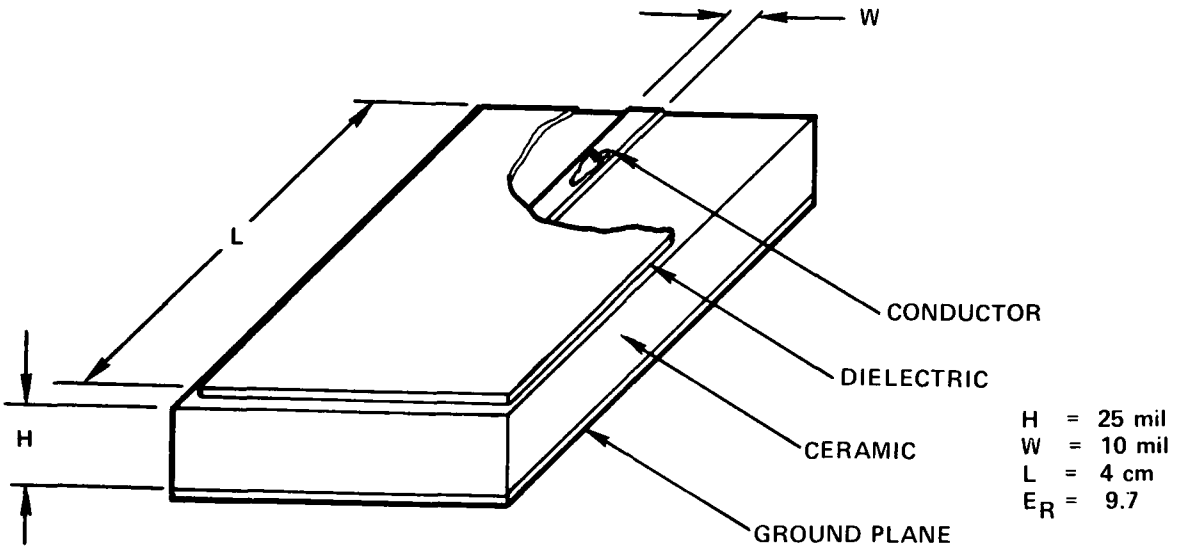


Figure 5-1 - Simple/Lumped Interconnect

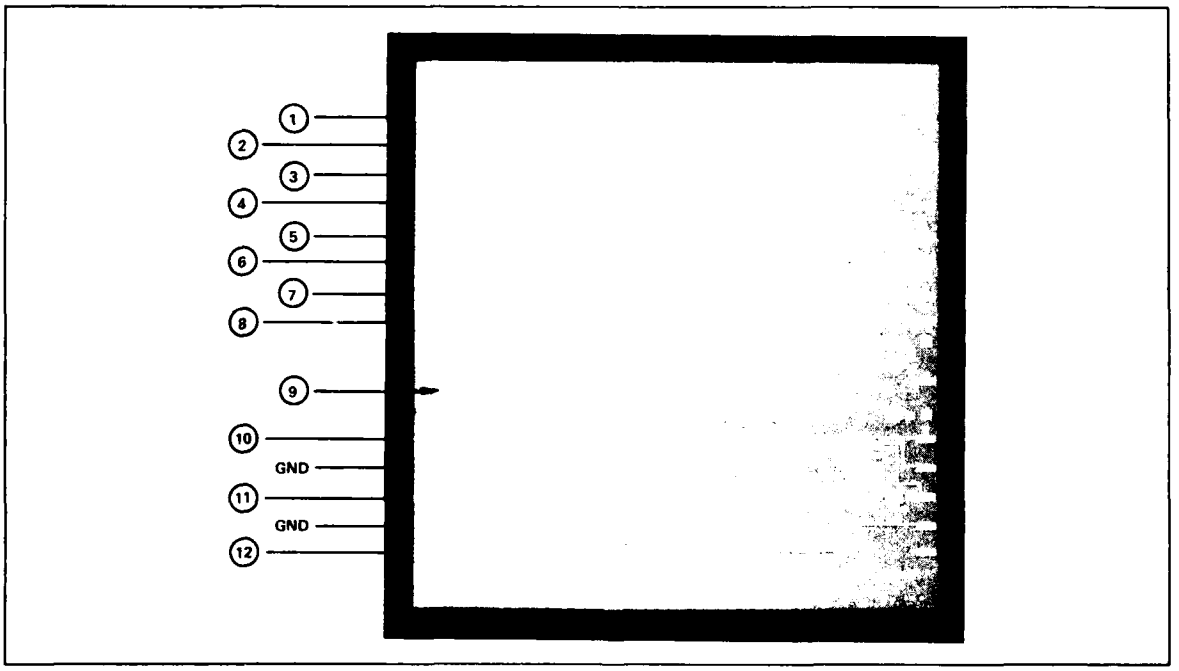


Figure 5-2 - First Interconnect Layer

5.2 Second Interconnect Layer

The following describes each pattern (See Figure 5-3).

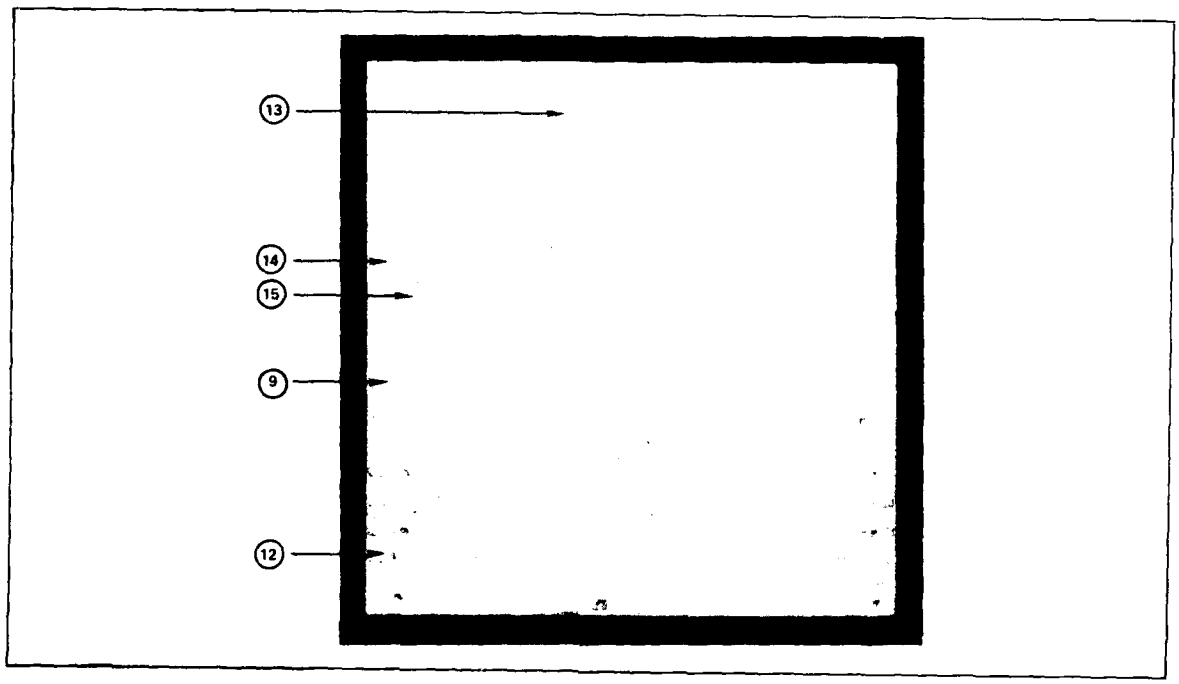


Figure 5-3 - Second Interconnect Layer

Pattern 13 - This pattern lies directly over the first three lines on the first interconnect layer. Provision has been made to ground this pattern using bond wires. Note that the pattern is made up of lines of three different lengths. All three lengths cross over line 1 on layer 1. Only the two longer lines cross over line 2, and line 3 has the longest line in the pattern crossing over it. The three lines on the first layer in conjunction with the pattern on the second layer are to be used in a crossover evaluation.

Line 14 - A single long interconnect.

Line 15 - This pattern is connected to ground and lies directly over line 7 on layer 1, converting line 7 from a microstrip to a stripline interconnect.

Line 9 - This completes the serpentine interconnection for via evaluation.

Line 12 - This completes the second serpentine interconnection.

Here again the large square at the bottom of the substrate forms one plate of a parallel plate capacitor.

5.3 Third Interconnect Layer

The interconnect pattern for this layer is identical to layer 1. However, the distance between an interconnect and the power plane approaches the interconnect line width. Although this interconnect is still considered simple/lumped, it is approaching a microstrip configuration. The purpose of each line is the same as was described for layer 1.

5.4 Power Plane

The power plane is located on top of the substrate. It is interdigitated as apparent in Figure 5-4. One set of fingers is ground, and the other set of fingers is power. This distributes power and ground over the hybrid for ease of chip power interconnection to pads on the top layer. It will be shown later that the spaces between the lines influence the electrical characteristics of the interconnection.

5.5 Sample Simulation

Line 1 on layer 1 was modeled and simulated. The simulated pulse response is compared to the pulse response data taken from the same line on the interconnection test substrate. For the simple/lumped configuration, the interconnect can be treated as part of a parallel plate capacitor because of the close proximity of the power plane. Since the dielectric is non-magnetic, the permeability of the medium can be considered to be that of free space. Knowing this, the inductance of the interconnect can be calculated. Once the inductance per unit length and capacitance per unit length are known, then the characteristic impedance of the interconnect can be determined. All of the values were calculated and are given in Figure 5-5.

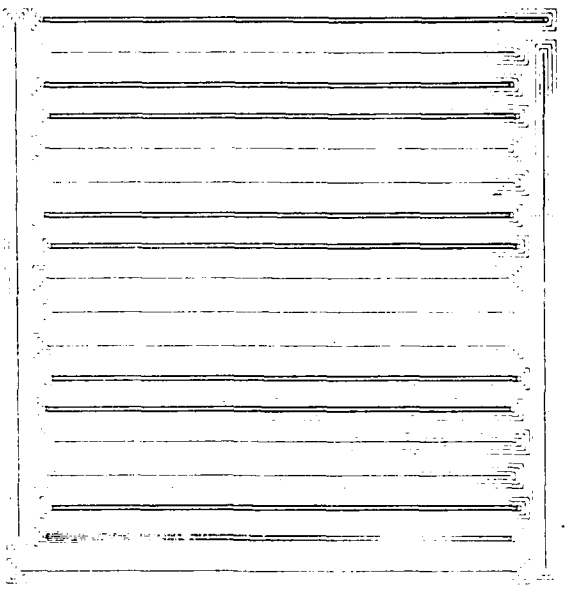


Figure 5-4 - Interdigitated Power Plane

$$C_{\ell}^{(2)} = \frac{\varepsilon_r \varepsilon_o A}{d} \qquad \text{where } A = \ell \times w = cm^2$$

$\varepsilon_r = 10$
$d = 2 \text{ mils} = 5.1 \times 10^{-3} \text{ cm}$ $\qquad A = 2.54 \times 10^{-2} \text{ cm} \times 1 \text{ cm}$
$w = 10 \text{ mils} = 2.54 \times 10^{-2} \text{ cm}$ $\qquad = 2.54 \times 10^{-2} \text{ cm}^2$
$\ell = 393.7 \text{ mil} = 1 \text{ cm}$
$\varepsilon_o = 8.85 \times 10^{-14} \text{ f/cm}$

$$C_{\ell} = \frac{10 \times 8.85 \times 10^{-14} \times 2.54 \times 10^{-2}}{5.1 \times 10^{-3}} = \frac{4.41 \text{ Pf/cm}}{}$$

$$L_{\ell}^{(2)} = \frac{\mu_o d}{w} \qquad \text{where } \mu_o = 4\pi \times 10^{-9}$$

$$L_{\ell} = \frac{4\pi \times 0.0^{-9} \times 5.1 \times 10^{-3}}{2.54 \times 10^{-2}} = \frac{2.52 \text{ nh/cm}}{}$$

$$R_{\ell} = \frac{0.055 \ \Omega/\text{cm}}{} \quad \text{(Calculated in Figure 2-4)}$$

$$Z_o = \sqrt{\frac{L}{C}} = \sqrt{\frac{2.52 \times 10^{-9}}{4.41 \times 10^{-12}}} = \frac{23.9 \ \Omega}{}$$

Figure 5-5 - Simple/Lumped Calculations

In order to be realistic the simulation must take into account the test interfaces. The model and interfaces are shown in Figure 5-6. The pulse rate was between 10 and 15 MHz and rise and fall time was 1 nsec. The coding is shown in Figure 5-7, while the pulse response, is shown in Figure 5-8. This plot will be compared to the actual test results.

5.6 Test Methods - Interconnection Test Substrate

There are two test methods that are employed in the evaluation of the interconnection test substrate. These are Time Domain Reflectometer (TDR) and time pulse response measurement.

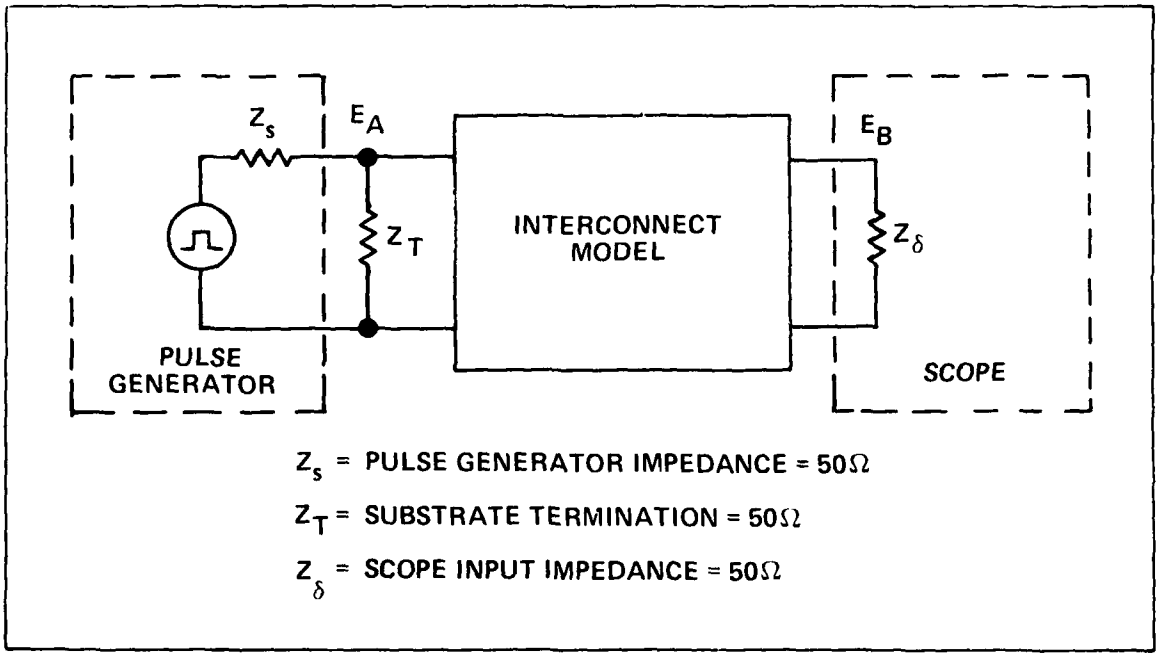


Figure 5-6 - Simple/Lumped Simulation

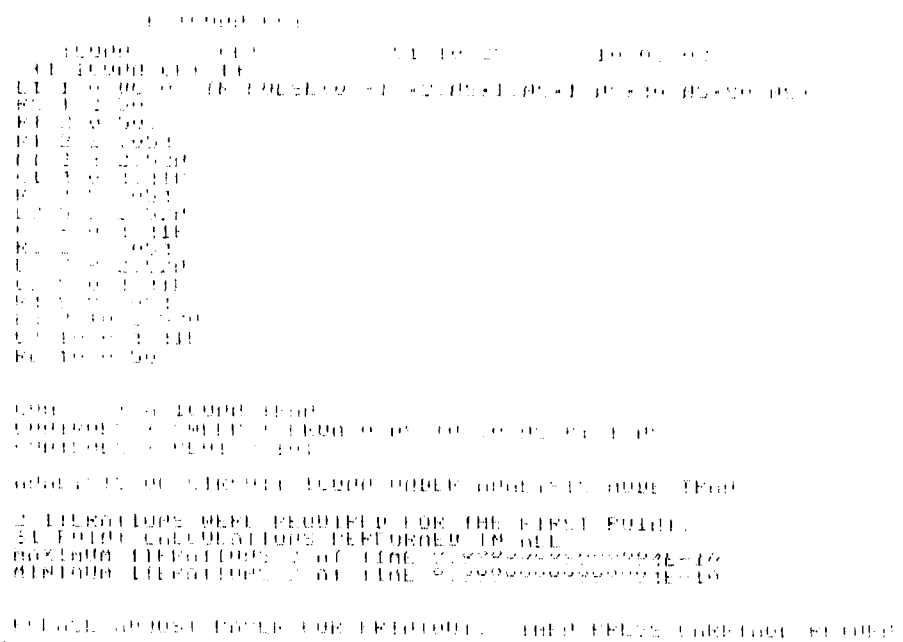


Figure 5-7 - Simple/Lumped Simulation Coding

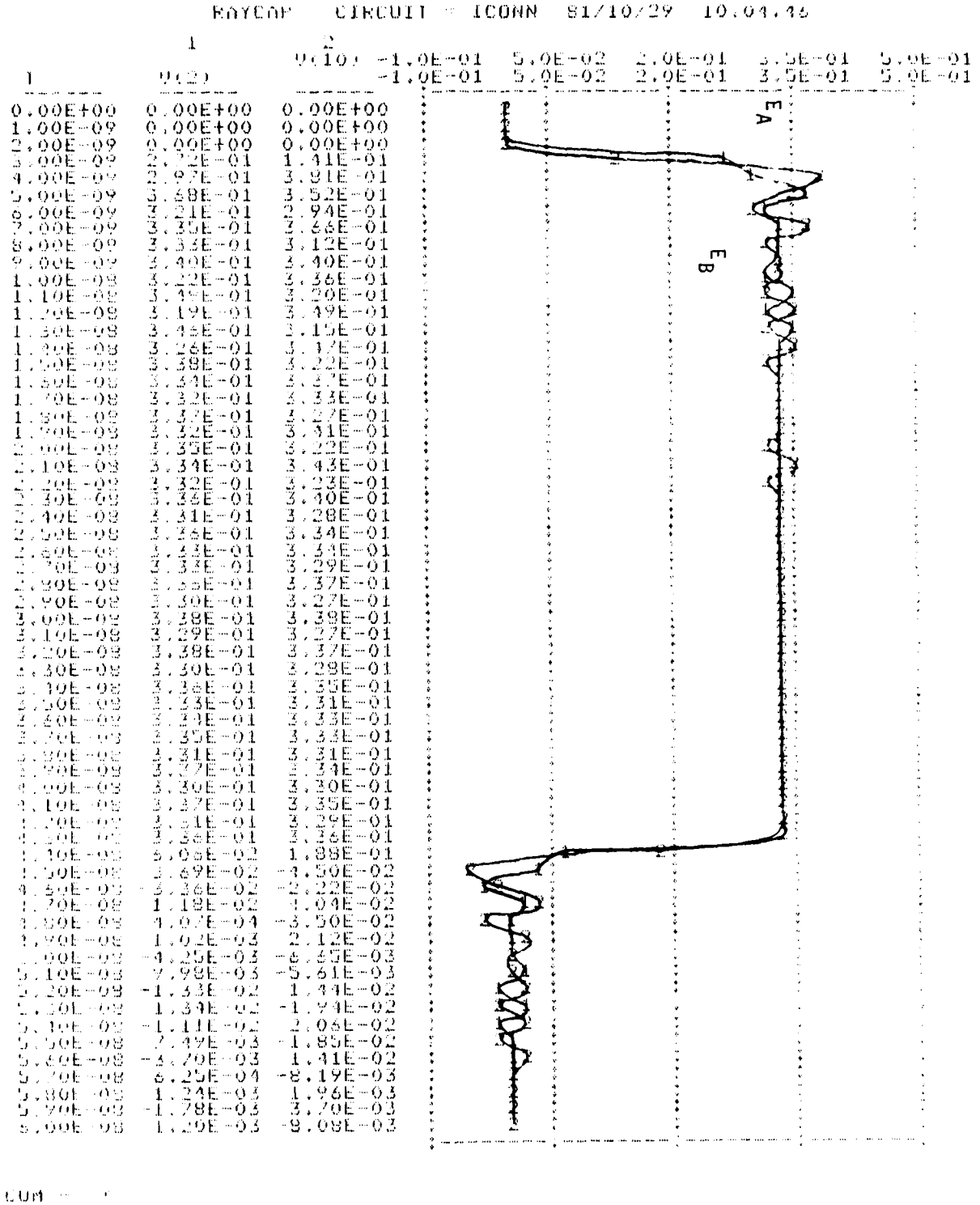


Figure 5-8 - Simple/Lumped Simulation Plot

5.6.1 Time Domain Reflectometer (TDR)

A TDR injects a pulse with a very fast rise time (45 psec) onto an interconnect and displays reflection coefficient (ρ) and two-way propagation delay time on a scope. Knowing the reflection coefficient, the characteristic impedance of the interconnect can be determined. Also, any discontinuties, capacitive or inductive, are displayed.

From transmission line theory an open line has a reflection coefficient of plus one. This means that a wavefront arriving at the open end of the line reflects in a positive direction at full amplitude. On the other hand, a short circuit at the end of line has a reflection coefficient of minus one. This means a wavefront will be reflected in a negative direction and at full amplitude. The formula used to calculate impedance from reflection coefficient follows.

$$Z_{Mea} = Z_{Ref} \frac{(1 + \rho)}{(1 - \rho)}$$

For an open $\rho = +1$

$$Z_{Mea} = Z_{Ref} \frac{(1 + 1)}{(1 - 1)} = \infty$$

For a short $\rho = -1$

$$Z_{Mea} = Z_{Ref} \frac{(1 - 1)}{(1-(-1))} = 0$$

5.6.2 Pulse Response

The effects of discontinuities, crossovers, capacitances, etc., will appear as pulse degradation including ringing and cross talk. Although pulse response will provide some insight as to the electrical effects of an interconnect, the exact performance cannot be determined. The actual response will be dependent upon the dynamic characteristics of the source and the load. However, TDR line measurement is a good tool to validate the computer interconnect model.

5.6.3 Test Interfaces

For high frequency digital measurements the interface between test equipment and hybrids must have precisely controlled impedances. Therefore, great care must be exercised when interfacing equipment, such as that shown in Figure 5-9. For example, to keep ground loops to a minimum when interfacing a pulse generator to a test substrate, a terminated coaxial cable must be used from the pulse generator. Otherwise, ringing will mask the measurement.

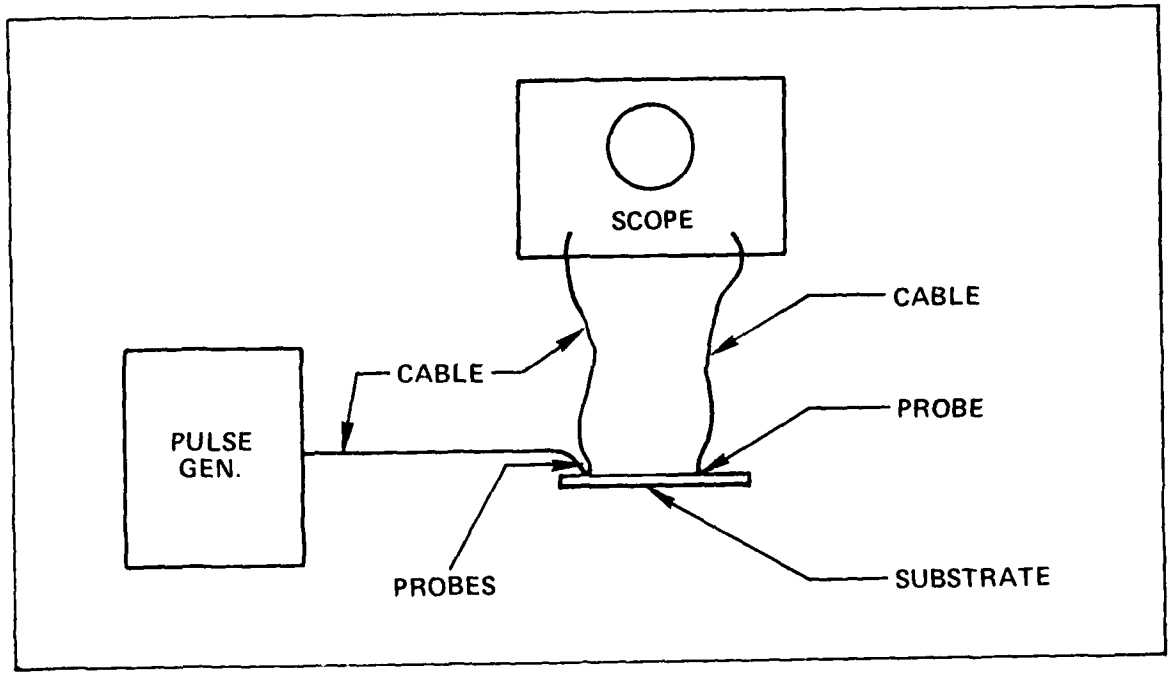


Figure 5-9 - Test Set-Up

5.6.4 Coaxial Probe

To get a pulse onto a substrate a newly developed probe was used. The shield or ground return is interfaced to the substrate via a second tip. A mechanical drawing of this probe is contained in Figure 5-10. Note that the tip that carries the shield to the substrate is helically wound to the probe shell.

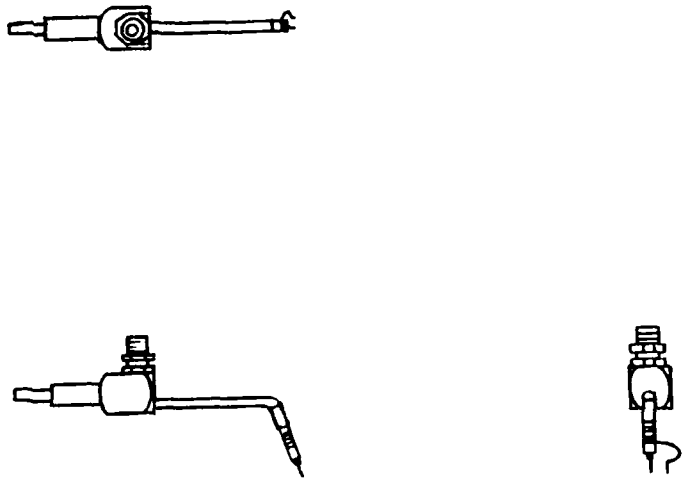


Figure 5-10 - 50Ω Coaxial Probe

The probe was evaluated using a *Tektronix* scope with 7S12 TDR plug-in. The plug-in contained a S-52 pulse generator and S-6 sampling head. The test set-up was as depicted in Figure 5-11. The results of a TDR measurement of the probe are shown in Figure 5-12. The discontinuity due to the SMA to BNC adapter is noted, as is the discontinuity due to the connector on the probe. Both discontinuities are capacitive.

To further evaluate the probe the tips were shorted together using a fuzz button. The fuzz button is simply a 2 mil gold bond wire rolled into a small sponge. The TDR response for this condition is shown in Figure 5-13. The first discontinuity noted is the result of the connector. The second discontinuity is the probe tip. Note that this discontinuity is inductive (inductive is positive while capacitive is negative). It was suspected that the inductance is caused by the outer tip which is wound in a helix. To verify this, a piece of 2 mil gold bond wire was wrapped around the shield of the probe and the center conductor where it emerges from the shield. The TDR response for this is shown in Figure 5-14. Notice that there is no inductive discontinuity, which verifies the suspicion.

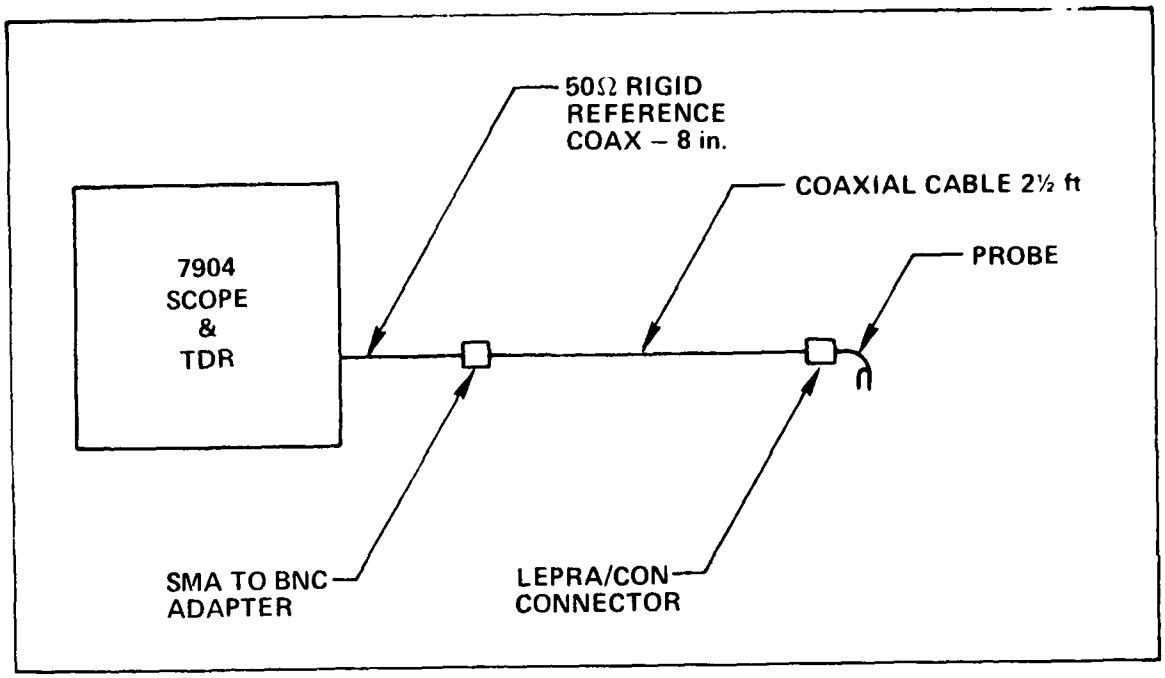
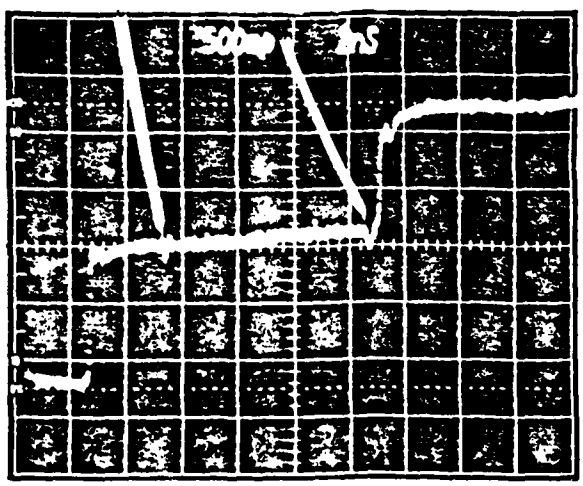


Figure 5-11 - Test Set-Up - Probe Evaluation

SMA TO BNC CONNECTOR PROBE



mρ

50Ω

nsec

Figure 5-12 - 50Ω Coaxial Probe and Cable (500 mρ/cm, 2 ns/cm)

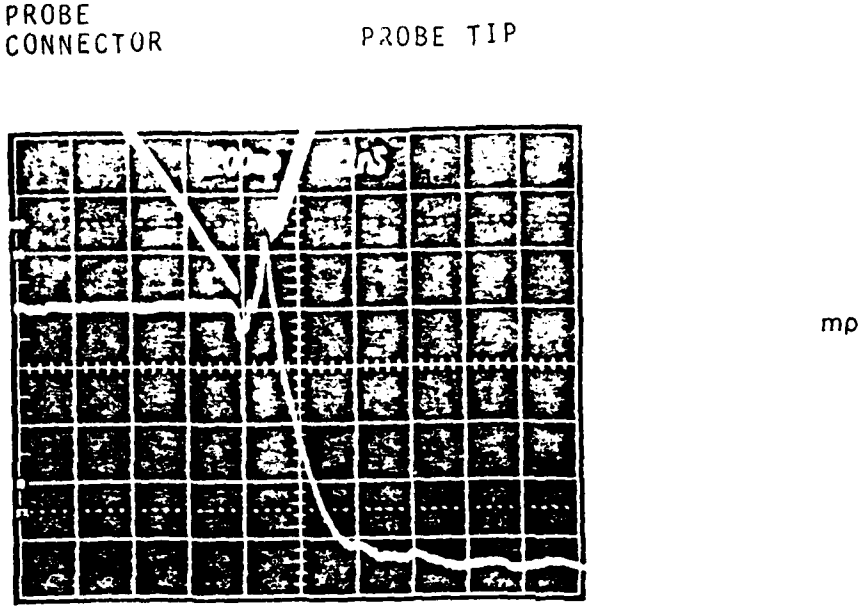


Figure 5-13 - Probe Shorted With Fuzz Button (200 mρ/cm. 1 ns/cm)

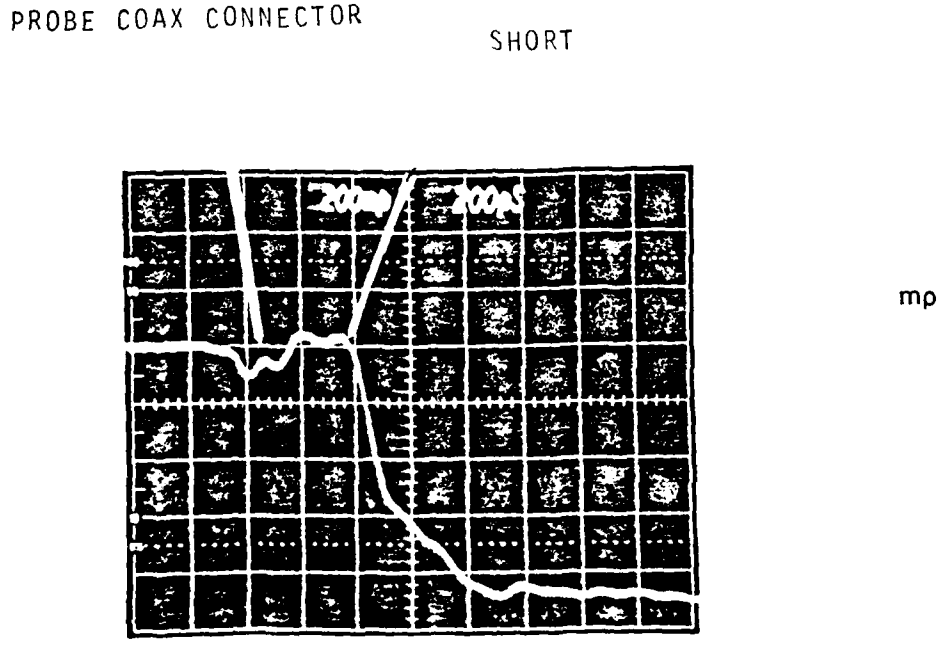


Figure 5-14 - Probe Shorted With Bond Wire (200 mρ/cm, 200 ps/cm)

This probe should be adequate for clock rates up to and beyond 250 MHz. However, for clock rates approaching the GHz range this probe will probably be inadequate. A special probe would have to be designed.

5.6.5 Test Substrate Evaluation

Three interconnection test substrate configurations were evaluated:

1) A single interconnect layer over a power plane
2) Two interconnect layers over a power plane
3) Three interconnect layers over a power plane

Each configuration was evaluated using TDR and pulse techniques.

5.6.5.1 First Layer Interconnect - TDR

A picture of the first interconnect layer was previously given in Figure 5-2. TDR measurements were performed on all but two lines, line 9 and 12. A large variation in the characteristic impedance along a single interconnect or from interconnect to interconnect was noticed, and Table 5-1 contains the reduced data. Note the large impedance variation on line 2, the reasons for which will be discussed later.

As was mentioned earlier in this report, a square parallel plate capacitor is located at the bottom of the interconnection test substrate. This capacitor measured 13.8 pf, which is much greater than the 8.8 pf calculated for a 2 mil thick dielectric. Refer to Figure 5-15 for the detailed calculation. Using the measured value, the dielectric thickness was calculated at 1.3 mils. Figure 5-16 contains this calculation. A variation of this magnitude in processing is considered normal. As a matter of fact, the measured variations in line characteristic impedance can be attributed to these normal variations in line width and dielectric thickness. Because of the close proximity of the power plane to the interconnect, variations in these parameters result in significant variations in impedance.

As mentioned earlier, line 2 exhibited a high impedance with large variations. This is evident from the TDR response in Figure 5-17. As a comparison, refer

TABLE 5-1

FIRST INTERCONNECT LAYER

Line No.	$Z_{o\ ave}$ (Ω)	$Z_{o\ low}$ (Ω)	$Z_{o\ high}$ (Ω)	C_t (pf)	C (pf/cm)	ℓ (cm)
1	19.4	17.6	21.9	34.5	6.2	4.57
2	LARGE VARIATION			29.4	4.8	4.83
3	30.0	28.1	33.3	35.7	5.5	5.33
4	32.0	29.4	34.7	13.8	6.5	1.65
5	20.4	18.0	21.4	23.5	6.2	3.3
6	37.0	33.3	40.1	32.7	5.2	4.83
7	34.7	30.0	42.6	41.0	6.2	5.59
8	34.7	31.3	37.0	35.2	6.0	4.83
10	30.0	21.4	40.9	31.0	5.4	4.57
11	28.1	26.9	34.7	35.6	5.4	5.33

CAP = 13.8 pf

NOTES: 1) Interdigitated power plane
2) Unterminated lines

$$C = \frac{\varepsilon_r \varepsilon_o A}{d}$$

where: $\varepsilon_r = 9.7$

$\varepsilon_o = 8.85 \times 10^{-14}$ f/cm

$A = \ell \times w$ where $\ell = 82$ mils $= 2.1 \times 10^{-1}$ cm

$w = 98$ mils $= 2.5 \times 10^{-1}$ cm

$d = 2$ mils $= 5.1 \times 10^{-3}$ cm

$A = 2.1 \times 10^{-1} \times 2.5 \times 10^{-1} = 5.2 \times 10^{-2}$ cm^2

$$C = \frac{9.7 \times 8.85 \times 10^{-14} \times 5.2 \times 10^{-2}}{5.1 \times 10^{-3}}$$

$C = \underline{8.8}$ pf

Figure 5-15 - Test Capacitor - 2 Mil Dielectric

$$C = \frac{\varepsilon_r \varepsilon_o A}{d}$$

$$d = \frac{\varepsilon_r \varepsilon_o A}{C_{MEA}}$$

where: $\varepsilon_r = 9.7$
$\varepsilon_o = 8.85 \times 10^{-14}$ f/cm
$A = 5.2 \times 10^{-2}$ cm^2
$C_{MEA} = 13.8$ pf

$$d = \frac{9.7 \times 8.85 \times 10^{-14} \times 5.2 \times 10^{-2}}{13.8 \times 10^{-12}}$$

$d = 3.3 \times 10^{-3}$ cm = 1.3 mils

Figure 5-16 - Test Capacitor Dielectric Thickness

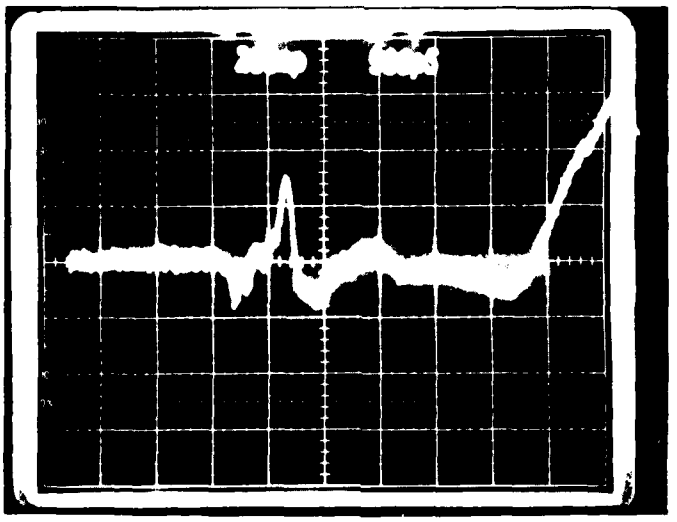


Figure 5-17 - Line 2 First Layer Interconnect - TDR Response

to Figure 5-18 which is the TDR response of line 1. This is the expected response. Inspection of the artwork revealed that line 2 did not lie directly over the power plane, but over a space on the interdigitated power plane. Because of this fact, impedance levels are dependent upon fringing effects.

To verify this, another substrate was fabricated, but this time with a solid ground plane. A TDR response of the same line, line 2, was as expected. This is shown in Figure 5-19.

If interconnects require a precisely controlled impedance, then the simple/lumped type construction should not be considered. Also, an interdigitated power plane in a microstrip configuration should not be used in applications requiring a controlled interconnect impedance.

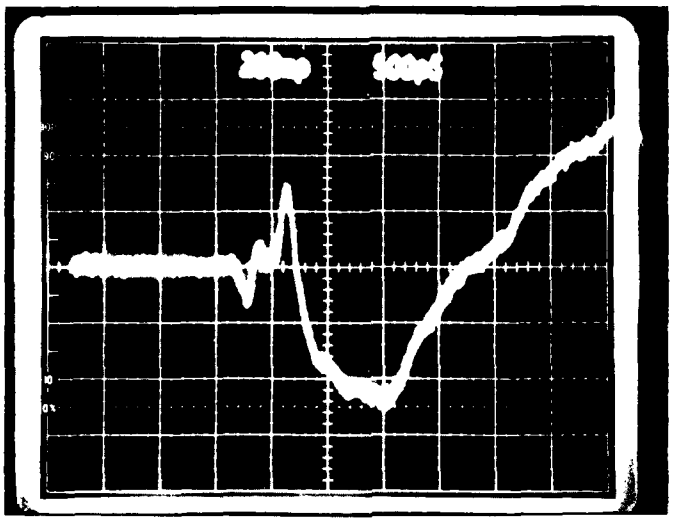
The TDR responses of the other lines for both the interdigitated and solid power planes are contained in Appendices A and B.

5.6.5.2 First Interconnect Layer - Pulse Response

The interconnects were pulsed at 15 MHz. The pulse rise and fall times were 1 nsec. Transmission line effects could be observed when viewing the input pulse at the pulse generator end. The coax cable from the pulse generator was terminated at the substrate end. However, the interface between the scope and the pulse generator was not. Since the pulse generator is properly terminated at the substrate end, these effects can be ignored.

Figure 5-20 shows the pulse response of line 1. Line 2, as discussed earlier, has a high and uncontrolled impedance which was also pulsed. The response for this line is given in Figure 5-21. As can be noted, the response for both lines is the same. The only degradation is in the rise and fall times. Observing the pulse response for the other lines, no real differences could be noted. From this we can conclude that for the frequencies of interest in this study the effects of 90^{o} and 45^{o} bends, impedance variations, etc., are negligible. For the simple/lumped type construction the large interconnect capacitance will have the greatest effect on the electrical performance of an interconnect. For the pulse response of the other lines see Appendix C.

50Ω

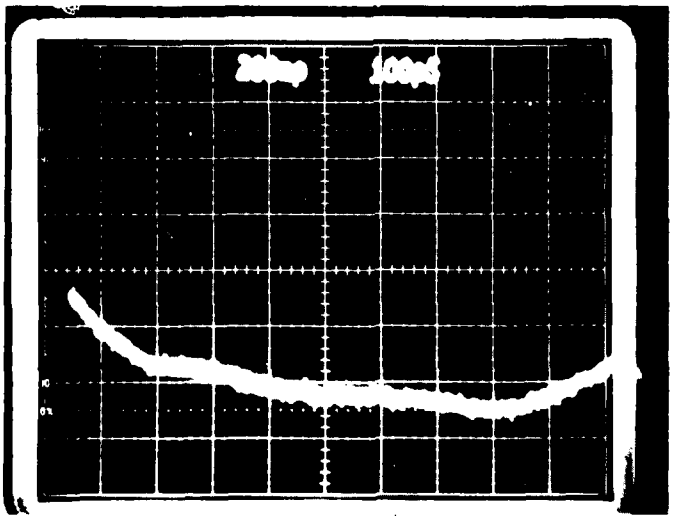


mρ

T = 500 ps/cm

INTERCONNECT

50Ω



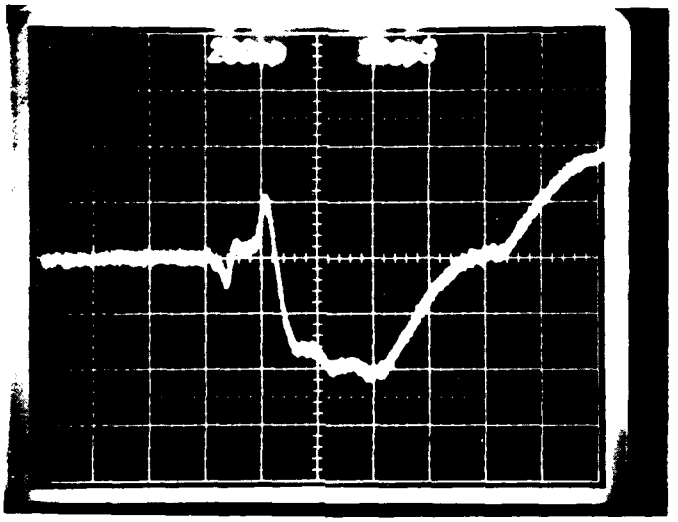
mρ

T = 100 ps/cm

INTERCONNECT

Figure 5-18 - Line 1 First Layer Interconnect - TDR Response

50Ω

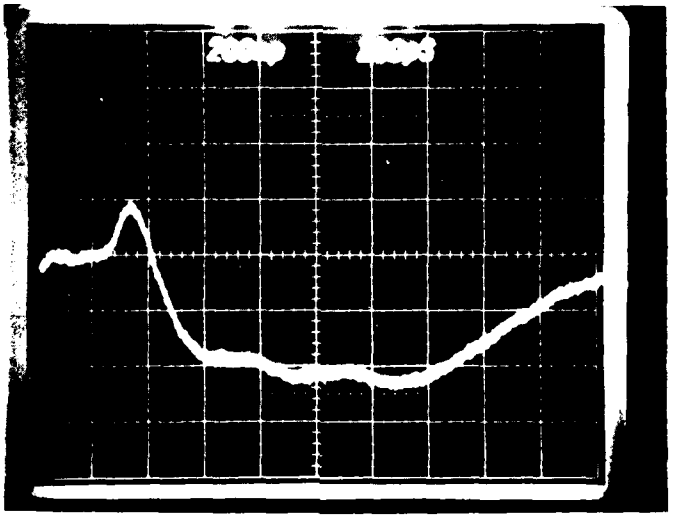


mρ

T = 500 ps/cm

INTERCONNECT

50Ω



mρ

T = 200 ps/cm

INTERCONNECT

Figure 5-19 - Line 2 First Layer Interconnect With Solid Ground Plane - TDR Response

INPUT

OUTPUT

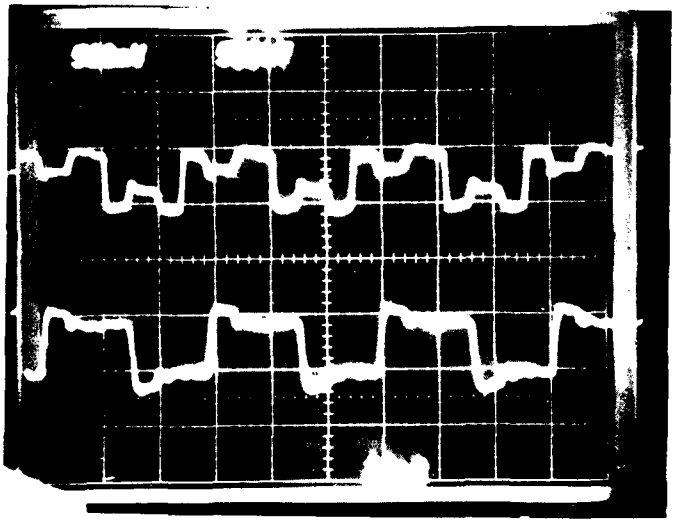


Figure 5-20 - Line 1 First Interconnect Layer

INPUT

OUTPUT

Figure 5-21 - Line 2 First Interconnect Layer

5.6.5.3 Scope Interface

As discussed in the previous section, transmission line effects were noted when making the pulse response measurements. These effects on the input end can be minimized by properly terminating the input at the substrate interface.

Figure 5-22 gives the pulse response of a line when the high impedance FET scope probe is used. The transmission line effects on the output pulse are due to the substrate to scope coaxial cable interface. These effects can be eliminated by removing the FET probe and feeding the signal directly into the 50 ohm scope input, as shown in Figure 5-23.

Although using the 50 ohm input of the scope terminates the cable, this is not a solution for all cases, specifically when observing CMOS/SOS outputs. This family cannot drive a 50 ohm load.

INPUT

OUTPUT

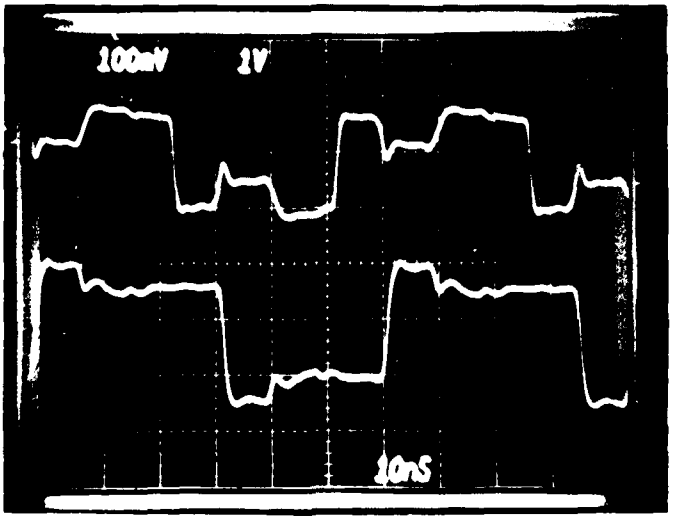


Figure 5-22 - FET Probe 10 MΩ Input

INPUT

OUTPUT

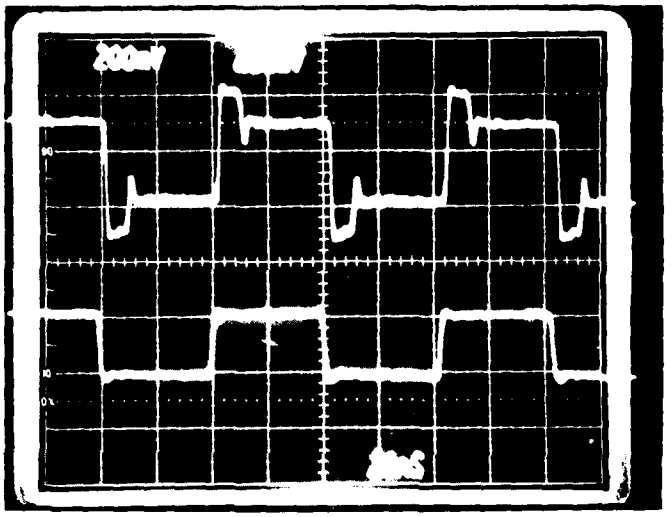


Figure 5-23 - 50Ω Scope Input

5.6.5.4 Cross Talk

The first three lines, Figure 5-24, were designed to evaluate long interconnects as well as cross talk. Lines 1 and 2 are on a 20 mil pitch, while lines 2 and 3 have a 30 mil pitch. This provides a means to evaluate cross talk for a number of different line spacing.

Cross talk measurements were made by pulsing one line and looking at an adjacent line. Both forward and backward cross talk was observed.

Forward cross talk is the noise that is coupled onto a line that propagates to the end of the line. However, not all the noise energy coupled in propagates to the output end of the line. Some of the energy propagates in the reverse direction to the input end of the line. This is defined as backward cross talk.

Line 1 was pulsed and the noise coupled onto line 3 was recorded. Figure 5-25 shows the forward cross talk. Figure 5-26 depicts the backward cross talk. In both cases the cross talk coupled was less than 10 percent of the pulse amplitude which is considered acceptable. Line 1 was pulsed and the coupling on line 2 was recorded. Here again the coupled noise was less than 10 percent of the pulsed voltage. See Figures 5-27 and 5-28.

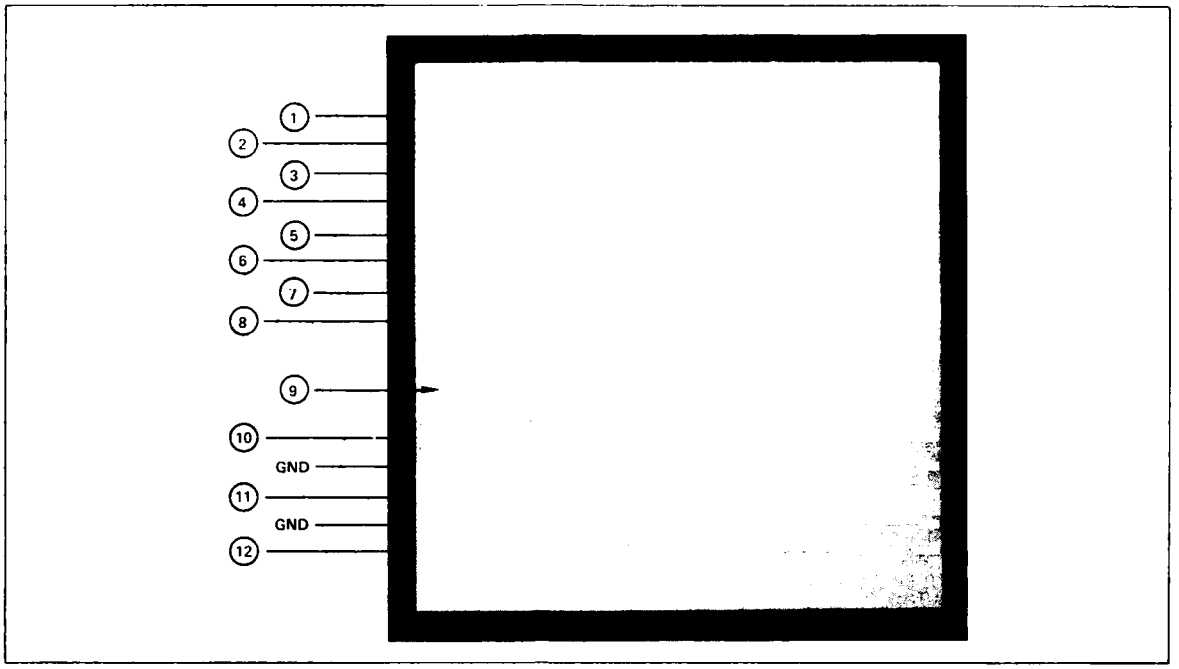


Figure 5-24 - First Interconnect Layer

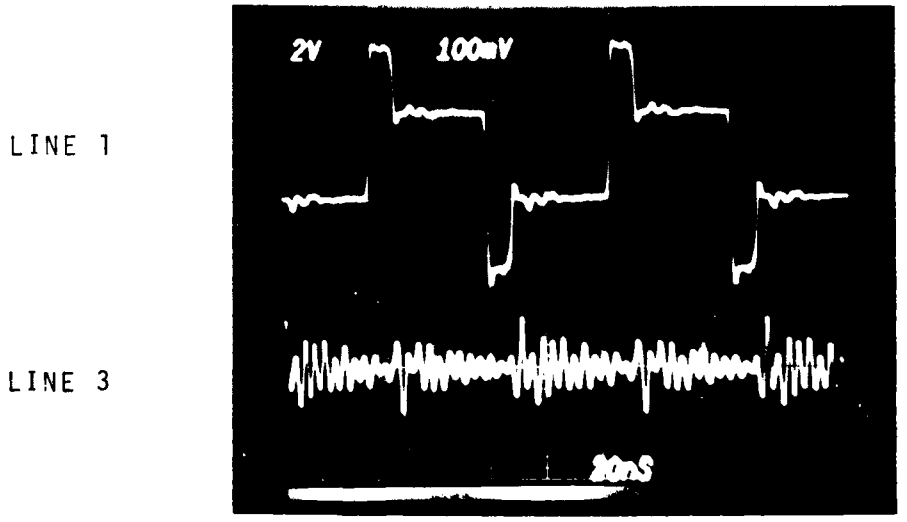


Figure 5-25 - Forward Cross Talk

LINE 1

LINE 3

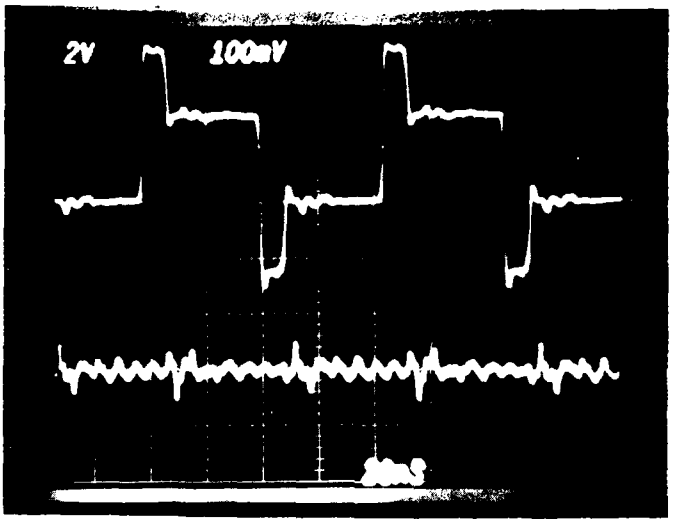


Figure 5-26 - Backward Cross Talk

LINE 1

LINE 2

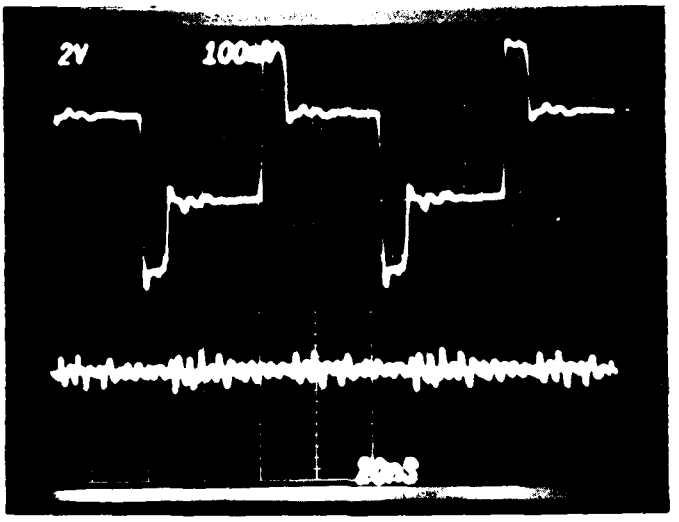


Figure 5-27 - Forward Cross Talk

Figure 5-28 - Backward Cross Talk

The cross talk levels were not predictable as expected for two reasons. First, because of the close proximity of the power plane to the interconnect and manufacturing tolerances large variations in electrical characteristics result. Secondly, line 2 was situated over a space in the power plane, resulting in very large impedance changes along the interconnect.

5.6.5.5 Second Interconnect Layer - TDR

Pattern 13 of Figure 5-29 is positioned over lines 1, 2 and 3 of the first interconnect layer for crossover evaluation. TDR measurements were made on lines 1, 2 and 3 with pattern 13 floating. Pattern 13 was grounded, and measurements were made again. The difference between the two sets of measurements is indicative of crossover effects.

Figure 5-30 is the TDR response of line 1 without crossovers while Figure 5-31 is the response with crossovers. Even though line 1 has the maximum number of crossovers, twenty, there are no discontinuities. Figures 5-32 and 5-33 are TDR responses of line 2 without and with crossovers. In this case the number of crossovers

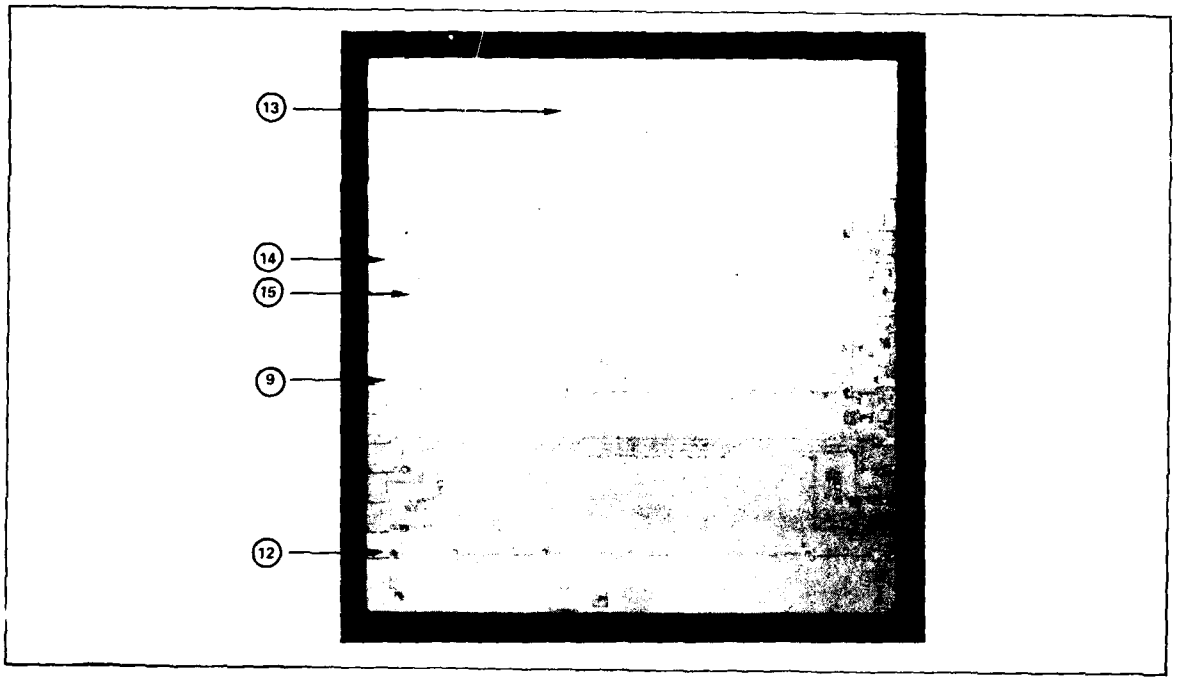


Figure 5-29 - Second Interconnect Layer

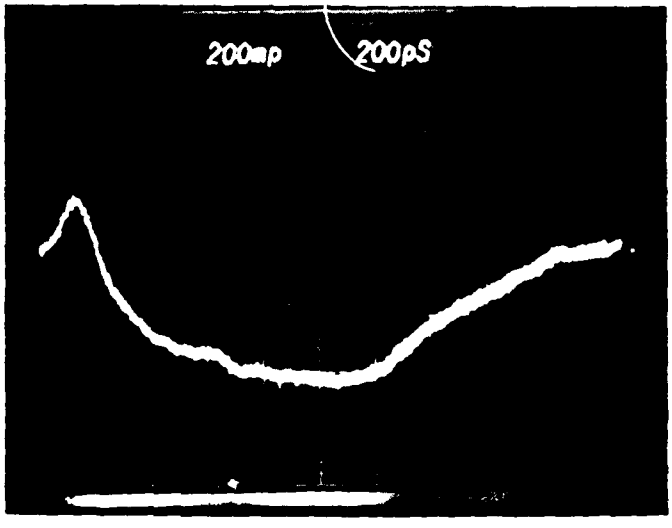


Figure 5-30 - Line 1 - Without Crossovers

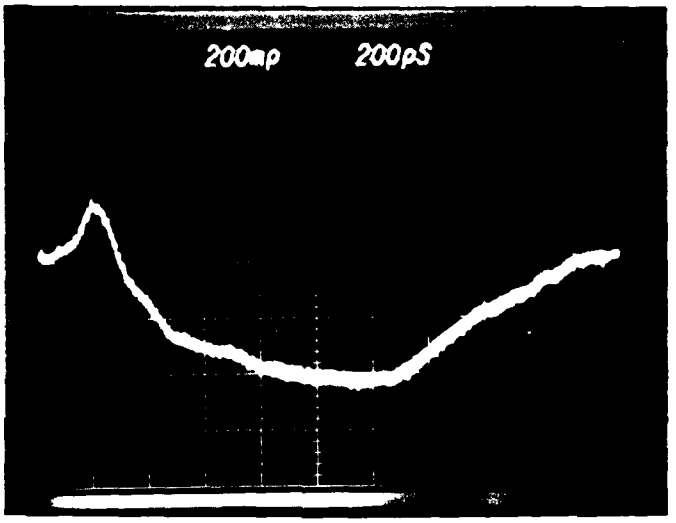


Figure 5-31 - Line 1 - With Crossovers

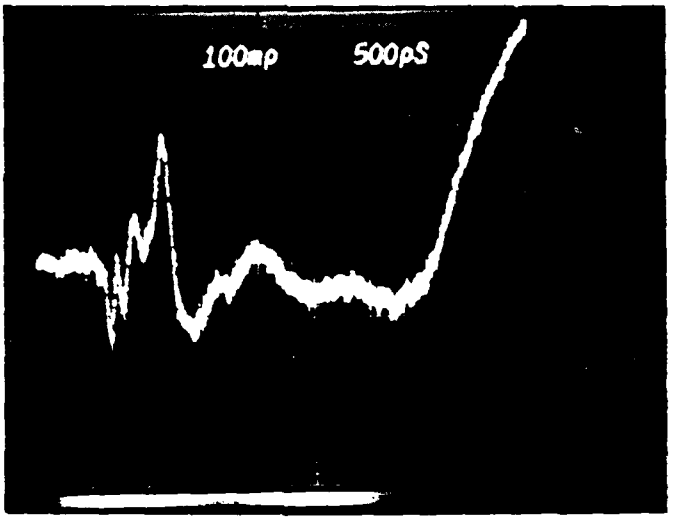


Figure 5-32 - Line 2 - Without Crossovers

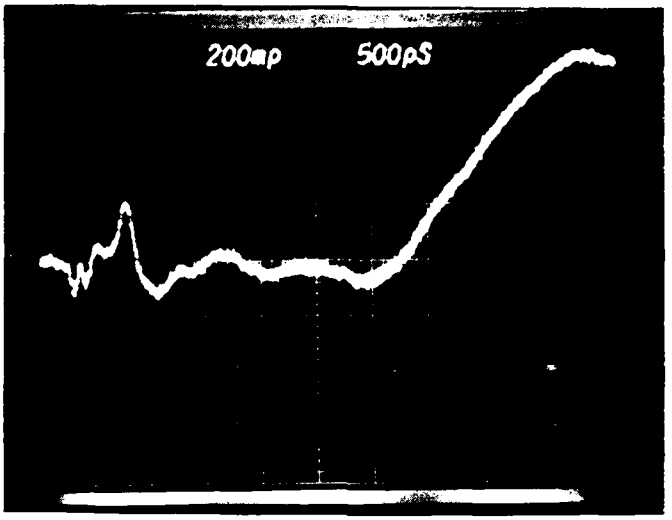


Figure 5-33 - Line 2 - With Crossovers

was 14. Here again are no observable effects due to the crossovers. Figures 5-34 and 5-35 are the responses for line 3. This interconnect has the least number of crossovers; and, as expected, there is no effect.

Figure 5-36 is the TDR response of line 14 of the second layer. The impedance of an interconnect on this layer should be higher than an equivalent interconnect on the first layer; and it is as it averages 33Ω. Line 15 is one plane of a stripline interconnect. The signal carrying conductor for this configuration is located directly below on layer 1. This line (15) is connected to ground. Figure 5-37 is the TDR response of the stripline interconnect. As expected the impedance is low, about 50Ω.

Figure 5-38 is the TDR response of line 9. This line is one of the serpentine interconnects and has ten vias. The other, line 12 with five vias, appears to have a defect. The large dip in the TDR response of Figure 5-39 represents a very low impedance. Since the variations in the TDR responses are not uniform and the vias are at uniform spacing, we can conclude that these variations are not due to vias.

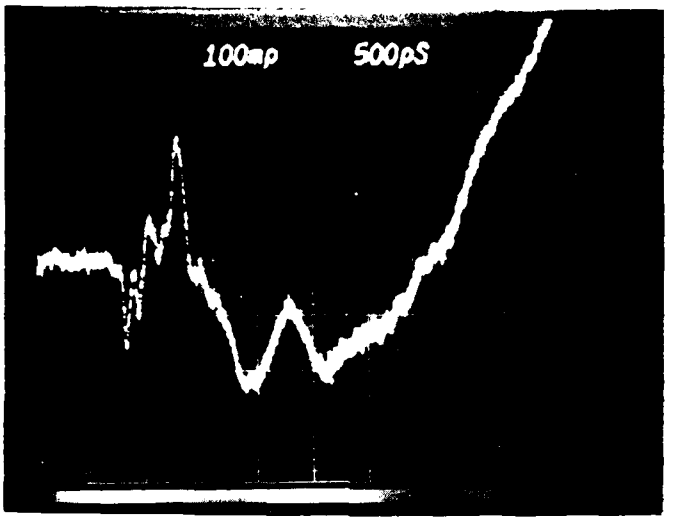


Figure 5-34 - Line 3 - Without Crossovers

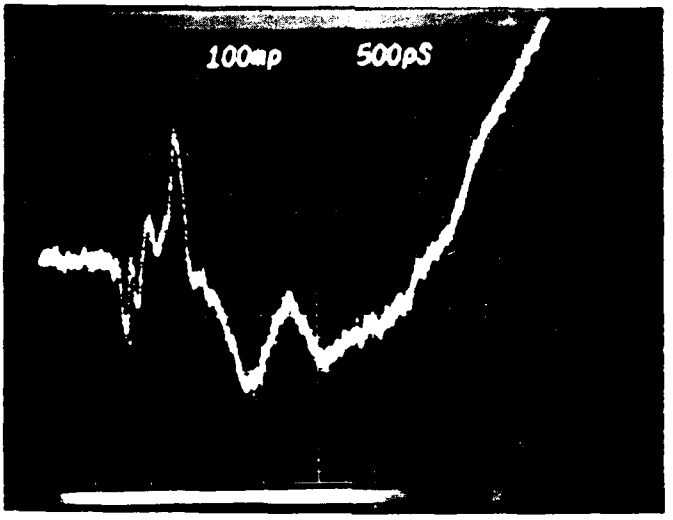


Figure 5-35 - Line 3 - With Crossovers

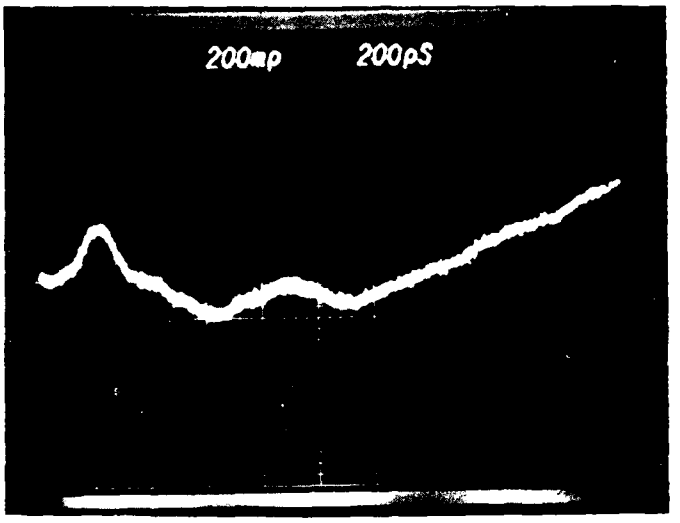


Figure 5-36 - Line 14 - Second Layer

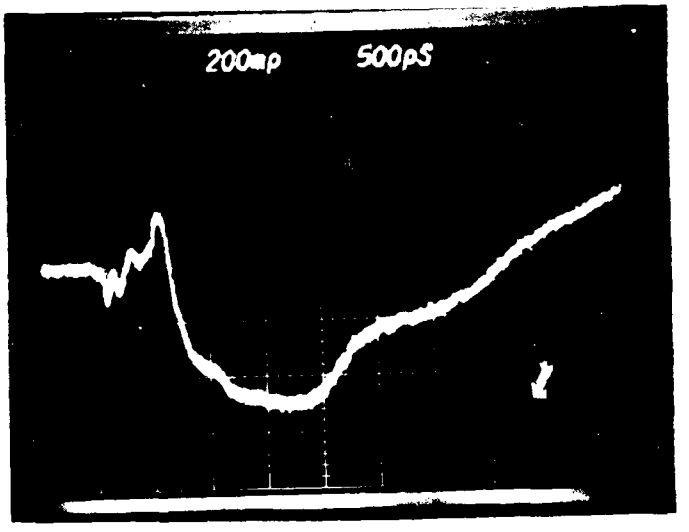


Figure 5-37 - Line 15 - Stripline

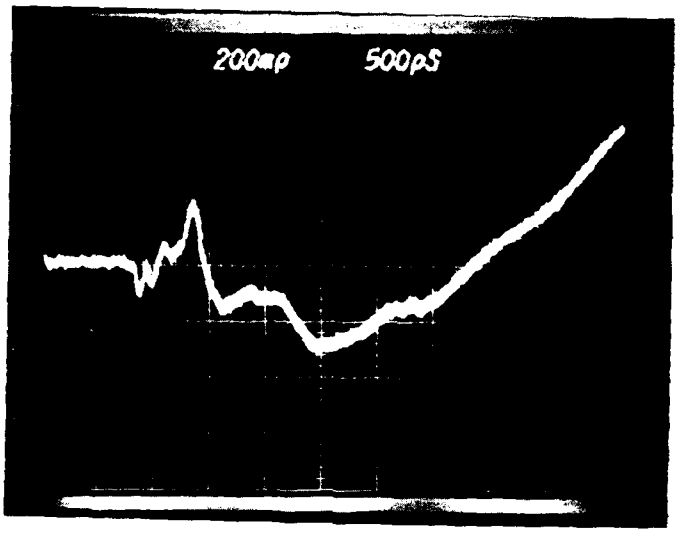


Figure 5-38 - Line 9 - Second Layer

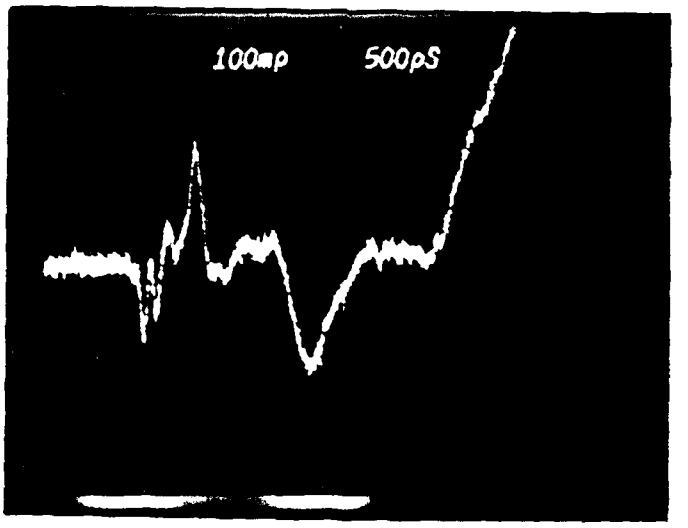


Figure 5-39 - Line 12 - Second Layer

5.6.5.6 Second Interconnect Layer - Pulse Response

The pulse responses of the interconnects of layer 1 showed little, if any, differences. Therefore, most of the data taken will appear in the Appendix A. However, the pulse response of line 1 without and with crossovers is of interest. These are given in Figures 5-40 and 5-41. As can be noted from the figures, both pulse responses are the same, which is to be expected as the TDR responses for the same set of conditions were identical.

5.7 Third Interconnect Layer - TDR

The interconnect pattern for this layer is the same as layer 1. Except for the magnitude of the characteristic impedance, the responses were not that much different. The impedances averaged 50 ohms. The types of variations observed in the first interconnect layer were evident in this layer. Just as variations in the first layer were due to manufacturing tolerances, the same is true for the third layer. One line, however, exhibited a

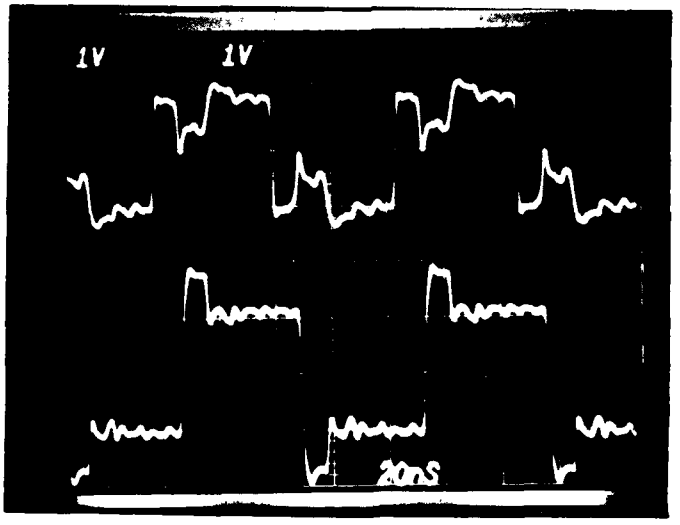


Figure 5-40 - Pulse Response Line 1 - Without Crossovers

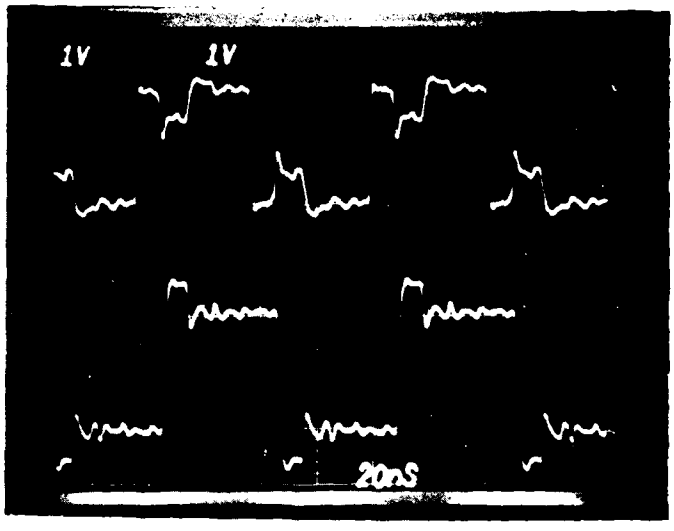


Figure 5-41 - Pulse Response Line 1 - With Crossovers

fairly even impedance profile, indicating that the overall line width and dielectric separations were relatively constant. The TDR responses for line 1 are shown in Figures 5-42 and 5-43.

A tabulation of the electrical characteristics for each of lines on this layer is given in Table 5-2. The remainder of the TDR response data taken for this layer is included in Appendix A.

5.7.1 *Third Interconnect Layer* - Pulse Response

The pulse response of the third layer interconnects are similar to those of layer 1. The one noticeable difference is that there is less degradation to the pulse edges because the interconnect capacitance is much lower. The capacitance per unit length is down by a factor of three. This can be observed by referring to Figures 5-44 and 5-45 which give the responses of lines 1 and 2. The pulse response data for the remaining lines are contained in Appendix A.

50Ω

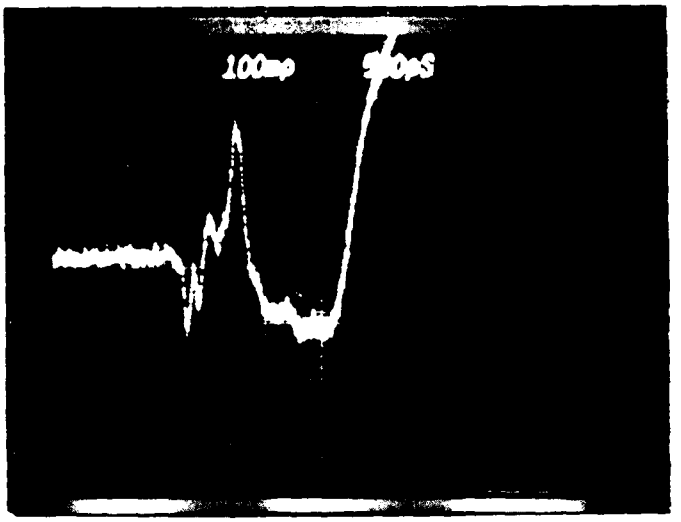


Figure 5-42 - Line 1 Third Layer

50Ω

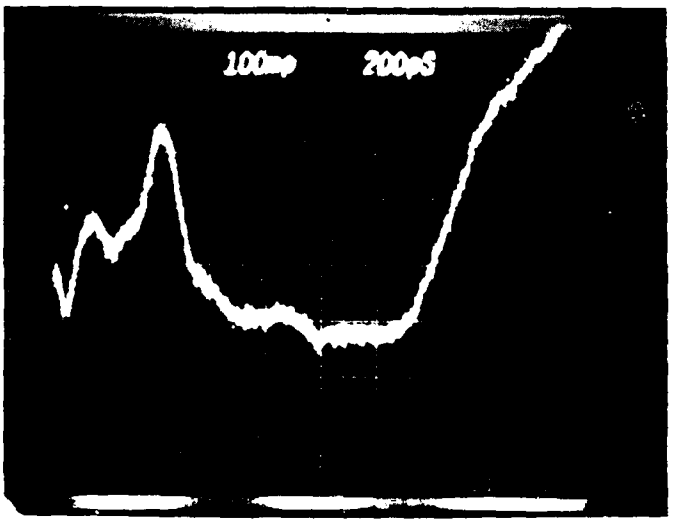


Figure 5-43 - Line 1 - Third Layer

AD-A114 437 RAYTHEON CO BEDFORD MA MISSILE SYSTEMS DIV F/G 9/5
TECHNICAL GUIDELINES FOR LSI HYBRID MICROCIRCUITS.(U)
DEC 81 C ROSS, J A CICCIO, R REGO DAAK20-80-C-0302
UNCLASSIFIED BR-13050 DELET-TR-80-0302 NL

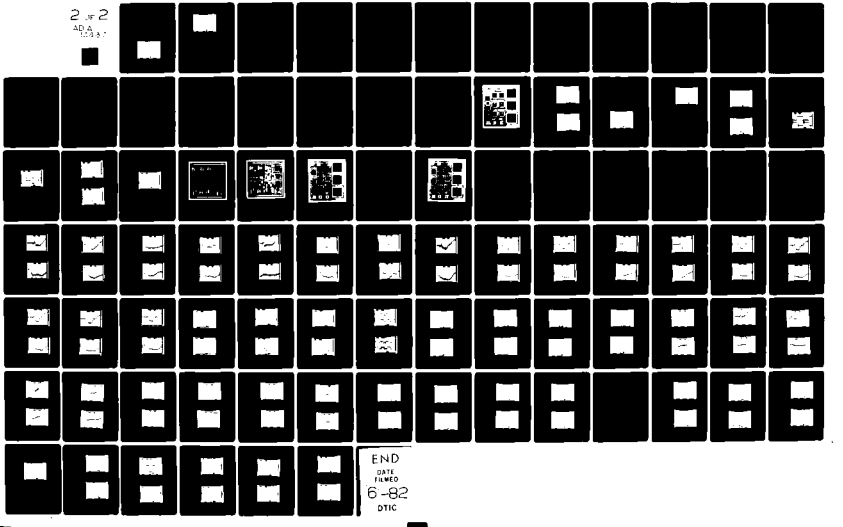


TABLE 5-2

THIRD INTERCONNECT LAYER

Line No.	$Z_{o\ ave}$ (Ω)	$Z_{o\ low}$ (Ω)	$Z_{o\ high}$ (Ω)	C_t (pf)	C (pf/cm)	ℓ (cm)
1	33.3	30.0	34.7	16.0	2.1	4.57
2	LARGE VARIATION			15.6	1.9	4.83
3	50.0	46.1	54.2	16.9	2.0	5.33
4	50.0	49.0	51.0	5.3	1.3	1.65
5	46.2	41.7	54.2	10.5	2.2	3.3
6	50.0	45.2	53.1	14.2	1.7	4.83
7	26.9	23.5	30.0	37.1	5.5	5.59
8	61.1	52.0	75.0	13.4	1.5	4.83
10	46.1	45.2	47.2	13.5	1.6	4.57
11	41.7	40.9	48.0	14.5	1.6	5.33

NOTES: 1) Interdigitated power plane
2) Unterminated lines

INPUT

OUTPUT

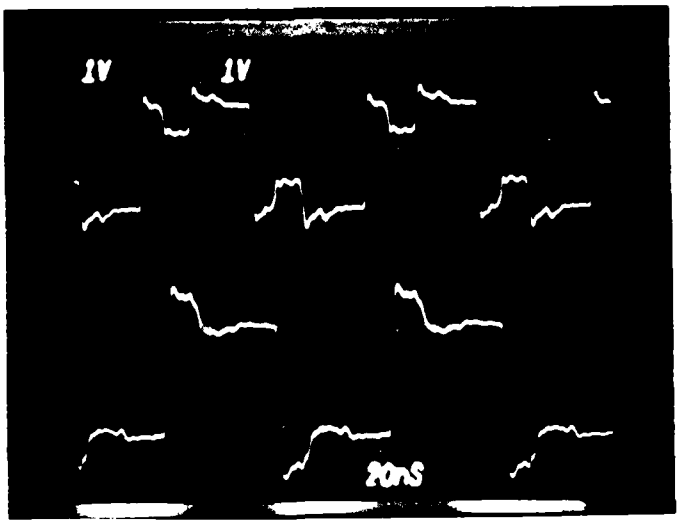


Figure 5-44 - Line 1 - Third Layer

INPUT

OUTPUT

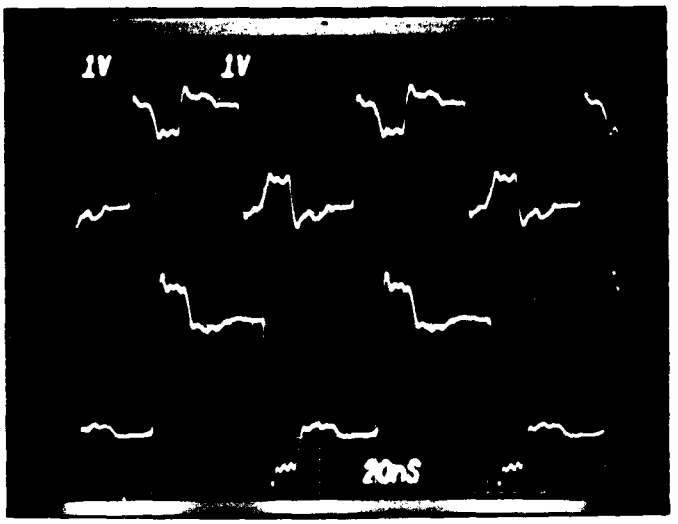


Figure 5-45 - Line 2 - Third Layer

5.8 Discussion

The simple/lumped construction, although the easiest to manufacture, does not provide well controlled electrical parameters. Impedance, capacitance and inductance variations are large. Even with these observed variations, there were no surprising discontinuities from the different interconnect configurations. The pulse response of each interconnect appeared to be the same, and 90 degree bends, vias, and crossovers, etc., had no noticeable effects.

Because of the large interconnect capacitance of the simple/lumped configuration, this type of interconnect may not be suitable for some logic families. The limited capacitive drive of the CMOS/SOS family will result in degraded performance. Even the ECL family will be affected because of increased propagation delay times. There will be some degradation in the performance of TTL, but it should not be significant.

The test interfaces were exercised, and some deficiencies were noted. The coaxial probe, providing it is terminated, is satisfactory. Also, for some families with low drive capability the output to scope interface will become a problem. This problem can be overcome in one of two ways: either by making the passive coaxial probe an active one, or by using a FET probe directly on the substrate for output measurements.

6. DIGITAL LOGIC FAMILIES

A number of logic families were considered for use in a test circuit that will serve to evaluate various types of hybrid construction. The types of construction are simple/lumped, microstrip and stripline. The logic families selected must be capable of operating at clock rates between 10 and 250 MHZ, with switching speeds up to 1 GHz.

6.1 Performance Characteristics

The performance characteristics of the following families were investigated and tabulated.

- TTL
- LSTTL
- STTL
- I^3L
- CMOS/Bulk
- CMOS/SOS
- ECL 10K
- ECL 100K

The tabulation appears as Table 6-1. In reviewing the table, it can be noted that the LS and S members of the TTL family cover the frequency range of 10 to 70 MHz. The I^3L family meets the requirements, but it was rejected because of lack of availability. The ECL family also operates within the frequency range of interest, but only 100K ECL will operate at 250 MHz. CMOS/Bulk was eliminated because it is too slow, as its maximum range is 6 MHz. CMOS/SOS was selected since it will operate in the MHz range, and devices manufactured at Raytheon were available.

Since the requirements are well defined (clock rates between 10 and 250 MHz, 1 GHz switching and production or near term production availability), these four families were selected:

1) LSTTL
2) STTL
3) CMOS/SOS
4) 100K ECL.

TABLE 6-1
PERFORMANCE CHARACTERISTICS

	TTL	STTL	LSTTL
Logic Levels	0/0V,1/5V	0/0V,1/5V	0/0V,1/5V
Noise Margins	400 mV	500 mV	500 mV
I_T(Current/Gate, Inverter)	2 mA	3.75 mA	0.4 mA
I_{OH}	-400 µA	-1000 µA	-400 µA
I_{OL}	16 mA	20 mA	4 mA
I_{IH}	40 µA	50 µA	20 µA
I_{IL}	-1.6 mA	-2.0 mA	-0.4 mA
T_P(Inverter-Internal+I/O)	T_{PLH} 22 ns at 15pF T_{PLH} 15 ns Internal Only 10 ns	T_{PLH} 4.5 ns T_{PLH} 5.0 ns INT. 3.0 ns	T_{PLH} 9.5 ns T_{PLH} 15 ns INT 9.5 ns
T_R	7 ns	2.5 ns	6 ns
T_F (I/O)	7 ns	2.5 ns	15 ns
Toggle Freq.(4 Bit Reg)	31 MHz	70 MHz	32 MHz
Supply Voltage	4.75-5.25V	4.75-5.25V	4.75-5.25V
Speed-Power	100 pJ	57 pJ	19 pJ
Available Functions	SSI,MSI,Memories, µProcessors,CGA's	SSI,MSI,Memories µProcessors,CGA's	SSI,MSI,Memories µProcessors,CGA's

TABLE 6-1 (Cont.)

Logic Levels Noise Margins	I^3L Same As LSTTL
I_{OH}	100 µA -400 µA
I_{OL}	4 µA
I_{IH}	20 µA
I_{IL}	-0.4 µA
T_P(Inverter)	6.0 ns (Internal At 100 µA)
T_R	0.6 ns
T_F	0.5 ns
Toggle Freq.	30-50 MHz
Supply Voltage	5V + Injection Current Source
Speed-PWR	0.15 pJ at 1 µA Cell Current
Available Functions	Configurable Gate Arrays

TABLE 6-1 (Cont.)

	100K ECL	10K ECL
Logic Levels	0/-1.705,1/-0.995	B: 0/-1.85,1/-0.96; A: 0/-1.65,1/-0.810
Noise Margins	125 mV	125 mV
I_T (Current Gate, Inverter)	-	-
I_{OL}	22 mA	22 mA
I_{IH}	250-550 µA	250-550 µA
I_{IL}	0.5 µA	0.5 µA
T_P (Inverter)	0.75 ns	2.0 ns
T_R (I/O)	0.70 ns	2.5 ns
T_F (I/O)	0.70 ns	2.5 ns
Toggle-Freq. (4-Bit Reg)	500 MHz	200 MHz
Supply Voltage	-4.5 V	-5.2 V
Speed-Power Product	60 pj	50 pj
Available Functions	SSI, MSI, (Gates, FF, etc.) Memories	SSI, MSI, (Gates, FFs etc.)

TABLE 6-1 (Cont.)

	CMOS (Bulk)	CMOS/SOS (Typical)
Logic Levels	0/0V 1/3-18V	0/0V, 1/3-15V
Noise Margins	At 5V 0.95V 10V 1.95V 15V 2.45V	1.0V at 5V and 10V
I_T (Current/Gate, Inverter)	At 5V (0.3 µA/kHz) f+I_{DD}/6 10V (0.6 µA/kHz) f+I_{DD}/6 15V (0.9 µA/kHz) f+I_{DD}/6	
I_{OH}	At 5V-0.88 (V_{OH} = 4.6) 10V-2.25 (V_{OH} = 9.5) mAdc 15V- 8.8 (V_{OH} = 13.5)	At 5V -2.1 mA 10V -3.3 mA 3ST. -3.8 mA
I_{OL}	At 5V 0.88 (V_{OH} = 0.4) 10V 2.25 (V_{OH} = 0.5) 15V 8.8 (V_{OH} = 1.5)	At 5V 2.8 mA 10V 2.8 mA 3ST 3.3 mA
I_{IH}	0.01 nAdc 0.3 µAdc	150 nA
I_{IL}	0.01 nAdc 0.3 µAdc	-1.3 nA
T_P (Inverter)	At 5V (0.90 ns/pF) C_L+20 ns 10V (0.36 ns/pF) C_L+22 ns 15V (0.26 ns/pF) C_L+17 ns	Internal Inverter/1.1-1.6 ns I/O Delay 15 ns at C_L = 30 pF --
T_R, T_F (I/O)	At 5V (1.35 ns/pF) C_L+32 ns 10V (0.6 ns/pF) C_L+20 ns 15V (0.4 ns/pF) C_L+20 ns	-- 5 ns at 25 pF --

TABLE 6-1 (Cont.)

	CMOS (Bulk)	CMOS/SOS (Typical)
Toggle Freq. (4-Bit Reg)	At 5V 1.8 MHz 10V 4.5 MHz 15V 6.0 MHz	> 70 MHz
Supply Voltage	3.0 to 18 Vdc	3.0 to 15 Vdc
Speed-Power Prod.	10 pH	--
Available Functions	SSI Gates, MSI, LSI, µProcessors, Memories	Custom VLSI, LSI and MSI, µProcessors (Very Limited)

6.2 Test Circuit

For this task a relatively simple test circuit is desired. This makes it easier to identify normal operation and degradation due to the electrical characteristics of interconnects. In addition, the duplication of the test circuit for each of the logic families is desirable because it provides a means of comparing one logic family with another.

A test circuit that will meet the above requirements is a four bit synchronous counter. Figure 6-1 depicts the test circuit for the 100K ECL family. The logic diagram is the same for the other families, therefore enhancing data correlation. Two gate elements are provided as a means to evaluate pulse degradation, resulting from a long interconnect and its restoration by a logic element.

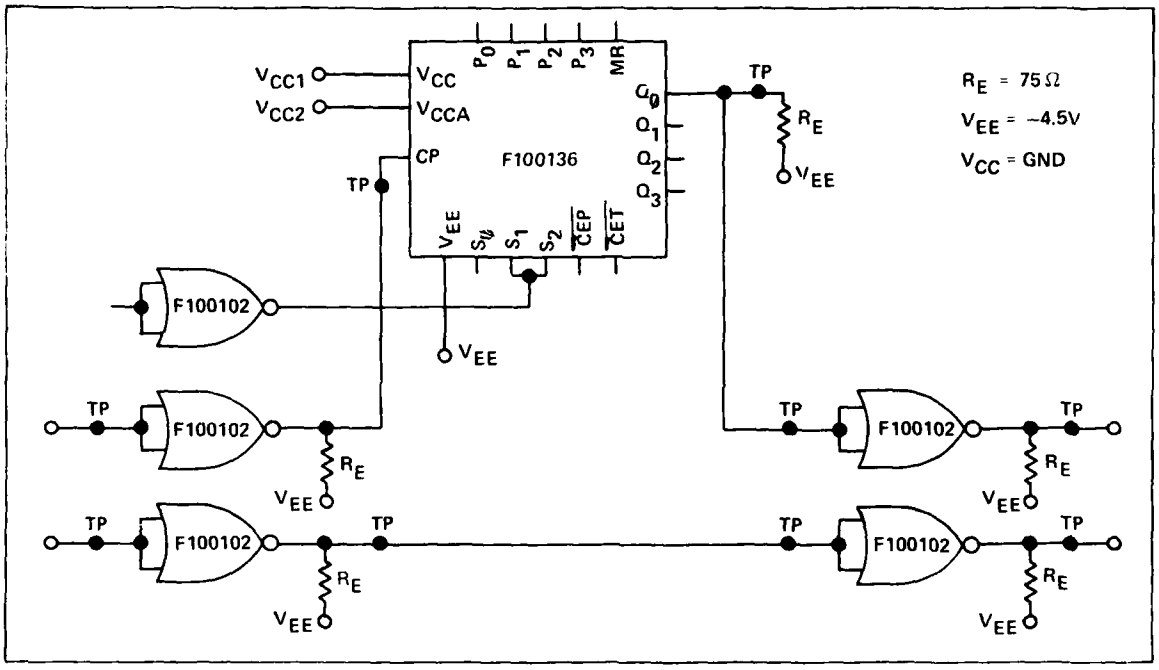


Figure 6-1 - Test Circuit - 100K ECL

7. MODELLING

Modelling the interconnect by themselves is not sufficient. The source and load should also be modelled since they will influence pulse response. All three models (source, load and interconnect) are to be interfaced and verified.

7.1 ECL Model

The output impedance of a 100K ECL logic element is 6 ohms at one level and 8 ohms at the other. Therefore a good source model is a voltage source with an output impedance of 7 ohms. The input impedance of an element is very high at low frequency. At high frequencies the input looks like a 2 picofarad capacitor.

7.2 CMOS/SOS Model

The test circuit for this family uses three RB917 CMOS/SOS chips. These chips were designed and fabricated at Raytheon, Bedford. The individual cells that make up this chip have been modelled in RAYCAP. These models were verified by comparing simulations to test data.

Figure 7-1 contains the schematic of the RB9050 driver cell. This is the model that will be used at the input end of a interconnect. Figure 7-2 shows the RB9020 clock input cell which represents the clock input to the counter. A gate input cell, RB9070 is shown in Figure 7-3. These three cells represent all of the RB917 interfaces with an interconnect.

7.3 Simulations

Since both the interconnect model and device model have been verified, all that remains is to mate the two and perform meaningful simulations. These simulations will be used as a basis for comparison with test data. Two configurations will be simulated: simple/lumped and microstrip. The simulation conditions and the points plotted (test points) are shown in Figure 7-4.

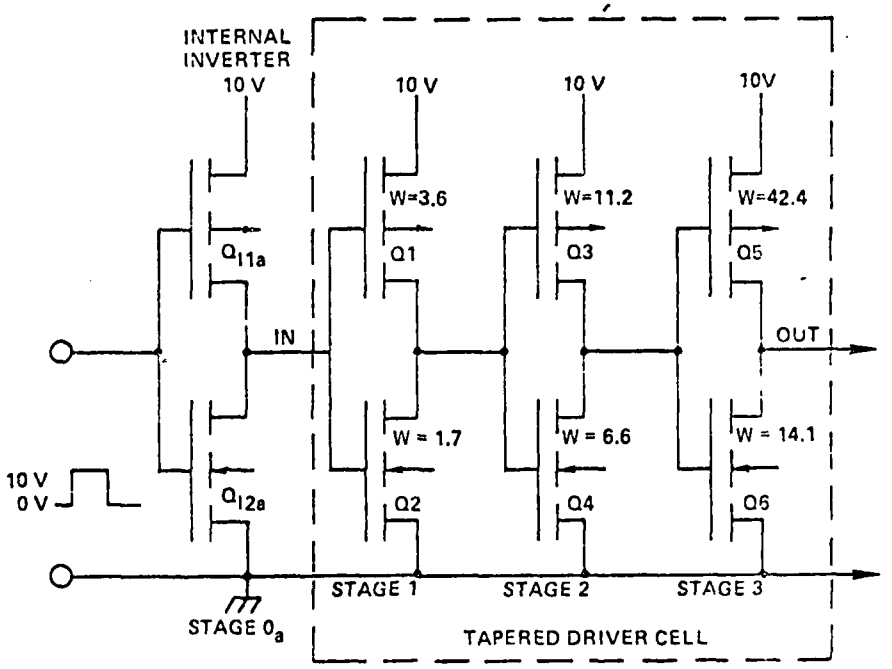


Figure 7-1 - RB-9050 Driver Cell

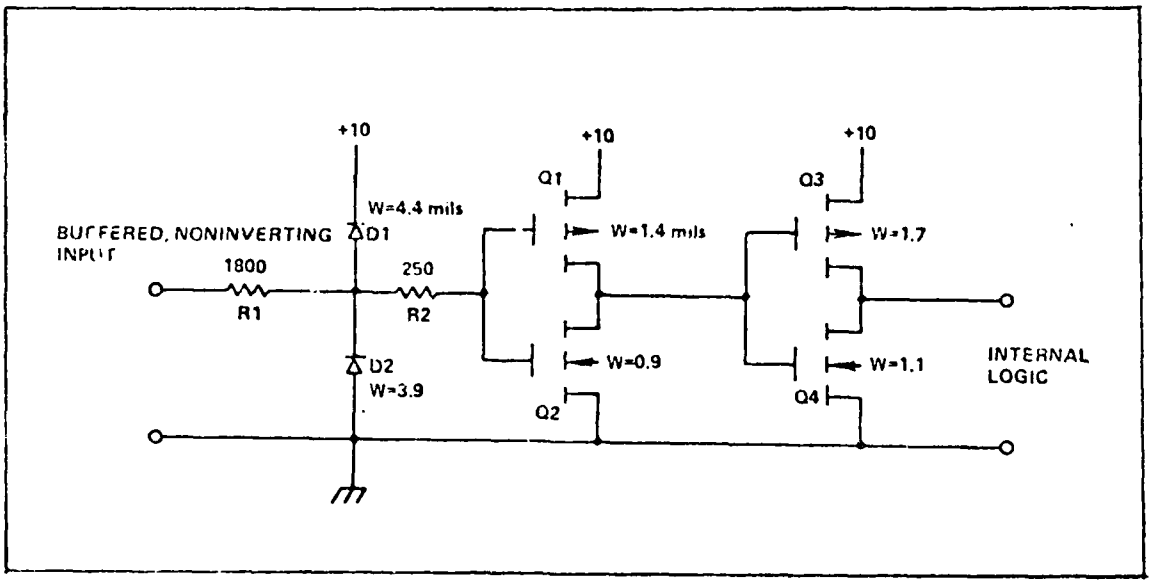


Figure 7-2 - RB-9020 Clock Input Cell

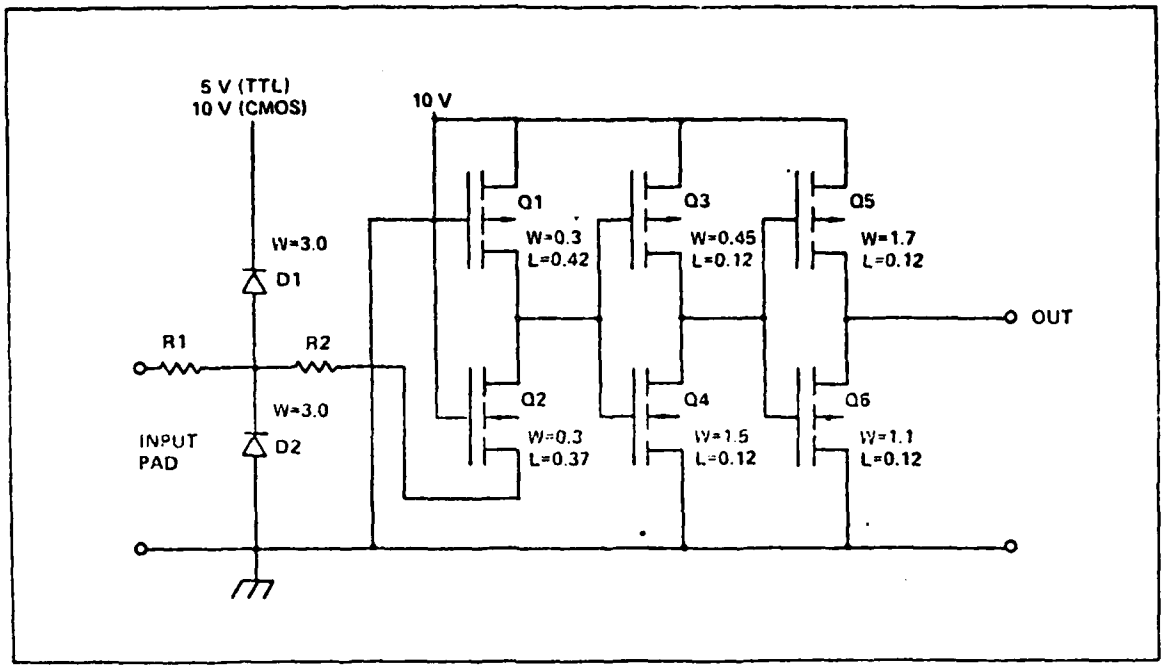
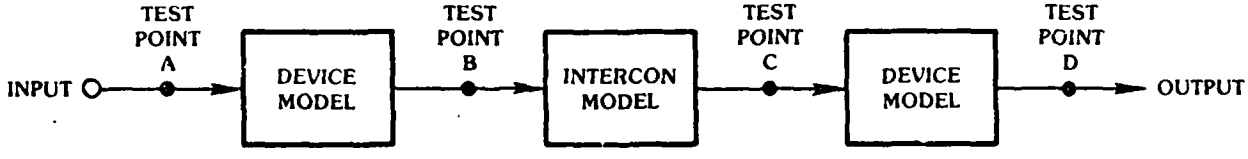


Figure 7-3 - RB9070 Gate Input Cell

SIMULATION MODEL



- CONDITIONS
  - MICROSTRIP
    - CMOS/SOS - 100 MHz CLOCK
  - SIMPLE/LUMPED
    - CMOS/SOS - 100 MHz CLOCK

Figure 7-4 - CMOS/SOS - Thick Film Interconnect Simulations

7.3.1 Simple/Lumped - CMOS/SOS

This configuration is characterized by low impedances and large interconnect capacitances. The RAYCAP coding for this simulation is given in Figure 7-5. The simulation plot of the input/output of the CMOS/SOS driver is shown in Figure 7-6. Note that the voltage at test point B does not go to zero after it switches from logic one. The plot of the input/output of the receiver at the end of the interconnect is given in Figure 7-7. Here again, the voltage at test point C does not go to zero and just barely crosses the device threshold. This results in a noise margin that is significantly reduced.

```
          P LIOS CKT
   LIOS        CKT          81/11/04.      14.33.15.
$$  LIOS CKT$$
E1  1  0 DC 10. TR PULSE(10.,0.,.2NS,1.NS,1.NS,5.NS,10.NS)
M1  2  0  1  3 RB9050A(25.)
E2  2  0 10.
R1  3  4 .054
L1  4  5 2.52N
C1  5  0 4.41P
R2  5  6 .054
L2  6  7 2.52N
C2  7  0 4.41P
R3  7  8 .054
L3  8  9 2.52N
C3  9  0 4.41P
R4  9 10 .054
L4 10 11 2.52N
C4 11  0 4.41P
M2  2  0 11 12 RB9020A(25.)

COM -  ? A LIOS TRAN
CONTROLS-? NOCONVERGE=150
CONTROLS-? SWEEP T FROM 0.NS TO 14.NS BY .2NS
CONTROLS-? SAVE V(1),V(3),V(11),V(12)$
CONTROLS-? PLOT 1 3*

ANALYSIS OF CIRCUIT LIOS UNDER ANALYSIS MODE TRAN
WITH THE FOLLOWING PARAMETERS SPECIFIED

NOCONVERGE =  1.50000E+02

87 ITERATIONS WERE REQUIRED FOR THE FIRST POINT.
71 POINT CALCULATIONS PERFORMED IN ALL
MAXIMUM ITERATIONS 53 AT TIME 1.19999999999986E-08
MINIMUM ITERATIONS 2 AT TIME 1.99999999999997E-10

PLEASE ADJUST PAPER FOR PRINTOUT.  THEN PRESS CARRIAGE RETURN.
?
```

Figure 7-5 - Coding Simple/Lumped - CMOS/SOS

RAYCAP CIRCUIT = LIOS 81/11/04 14.38.41

T	V(1)	V(3)
0.00E+00	1.00E+01	5.92E-05
2.00E-10	1.00E+01	5.92E-05
4.00E-10	8.00E+00	-3.04E-04
6.00E-10	6.00E+00	1.24E-03
8.00E-10	4.00E+00	1.20E-03
1.00E-09	2.00E+00	3.10E-03
1.20E-09	1.71E-13	-1.07E-02
1.40E-09	0.00E+00	-3.23E-02
1.60E-09	0.00E+00	1.21E-01
1.80E-09	0.00E+00	9.07E-01
2.00E-09	0.00E+00	1.05E+00
2.20E-09	0.00E+00	1.27E+00
2.40E-09	0.00E+00	1.50E+00
2.60E-09	0.00E+00	1.79E+00
2.80E-09	0.00E+00	2.75E+00
3.00E-09	0.00E+00	3.29E+00
3.20E-09	0.00E+00	3.93E+00
3.40E-09	0.00E+00	3.87E+00
3.60E-09	0.00E+00	4.15E+00
3.80E-09	0.00E+00	4.75E+00
4.00E-09	0.00E+00	5.42E+00
4.20E-09	0.00E+00	5.62E+00
4.40E-09	0.00E+00	5.63E+00
4.60E-09	0.00E+00	5.88E+00
4.80E-09	0.00E+00	6.28E+00
5.00E-09	0.00E+00	6.70E+00
5.20E-09	0.00E+00	6.92E+00
5.40E-09	0.00E+00	6.95E+00
5.60E-09	0.00E+00	6.98E+00
5.80E-09	0.00E+00	7.32E+00
6.00E-09	0.00E+00	7.74E+00
6.20E-09	0.00E+00	7.82E+00
6.40E-09	2.00E+00	7.76E+00
6.60E-09	4.00E+00	7.89E+00
6.80E-09	6.00E+00	8.13E+00
7.00E-09	8.00E+00	8.31E+00
7.20E-09	1.00E+01	8.48E+00
7.40E-09	1.00E+01	8.49E+00
7.60E-09	1.00E+01	8.48E+00
7.80E-09	1.00E+01	8.47E+00
8.00E-09	1.00E+01	8.29E+00
8.20E-09	1.00E+01	8.05E+00
8.40E-09	1.00E+01	7.52E+00
8.60E-09	1.00E+01	7.80E+00
8.80E-09	1.00E+01	7.12E+00
9.00E-09	1.00E+01	7.03E+00
9.20E-09	1.00E+01	6.02E+00
9.40E-09	1.00E+01	5.77E+00
9.60E-09	1.00E+01	5.35E+00
9.80E-09	1.00E+01	5.28E+00
1.00E-08	1.00E+01	4.96E+00
1.02E-08	1.00E+01	4.36E+00
1.04E-08	8.00E+00	3.96E+00
1.06E-08	6.00E+00	3.80E+00
1.08E-08	4.00E+00	3.79E+00
1.10E-08	2.00E+00	3.43E+00
1.12E-08	1.07E-11	3.06E+00
1.14E-08	0.00E+00	2.79E+00
1.16E-08	0.00E+00	2.85E+00
1.18E-08	0.00E+00	3.60E+00
1.20E-08	0.00E+00	3.51E+00
1.22E-08	0.00E+00	3.55E+00
1.24E-08	0.00E+00	3.37E+00
1.26E-08	0.00E+00	3.85E+00
1.28E-08	0.00E+00	4.70E+00
1.30E-08	0.00E+00	5.14E+00
1.32E-08	0.00E+00	5.45E+00
1.34E-08	0.00E+00	5.28E+00
1.36E-08	0.00E+00	5.54E+00
1.38E-08	0.00E+00	6.15E+00
1.40E-08	0.00E+00	6.76E+00

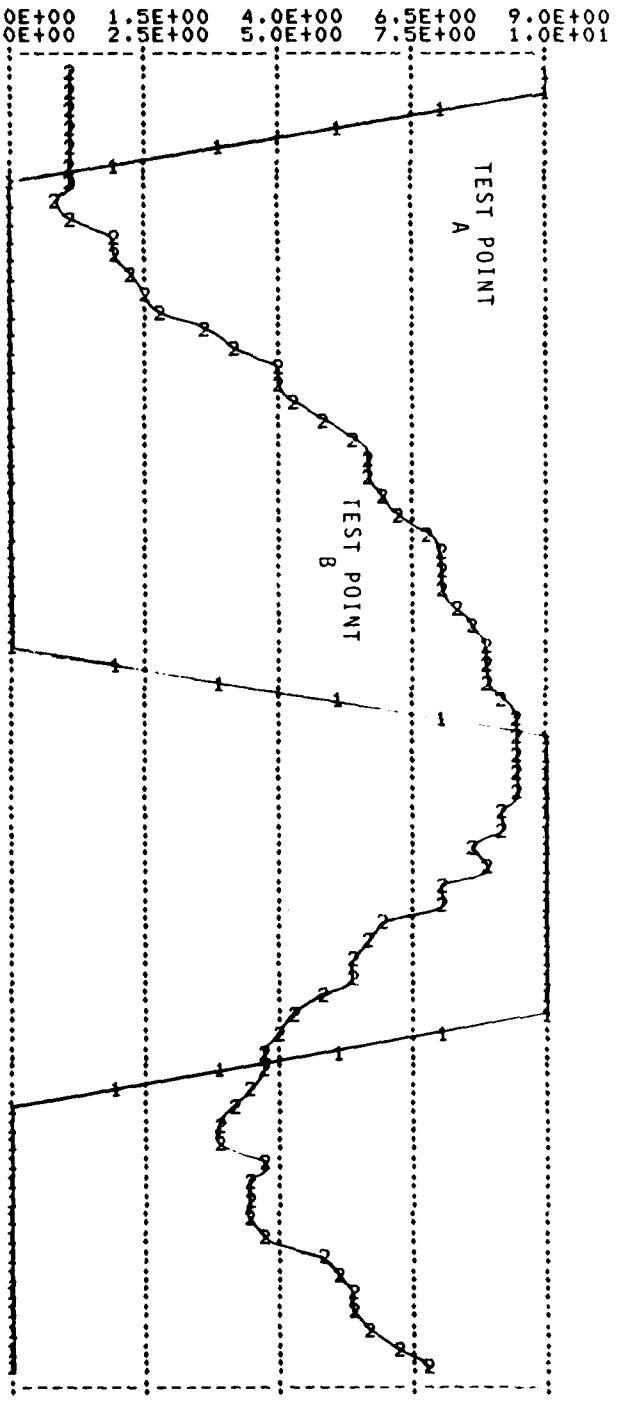


Figure 7-6 - CMOS/SOS Driver Input/Output - Simple/Lumped

RAYCAP CIRCUIT = LIOS 81/11/04 14.40.27

T	1 V(11)	2 V(12)
0.00E+00	5.92E-05	1.78E-04
2.00E-10	5.92E-05	1.78E-04
4.00E-10	5.06E-05	1.78E-04
6.00E-10	1.89E-05	1.78E-04
8.00E-10	8.69E-05	1.79E-04
1.00E-09	7.14E-04	1.84E-04
1.20E-09	1.99E-03	1.87E-04
1.40E-09	1.02E-03	1.62E-04
1.60E-09	-6.32E-03	1.13E-04
1.80E-09	1.47E-02	4.08E-04
2.00E-09	2.29E-01	2.06E-03
2.20E-09	8.76E-01	5.09E-03
2.40E-09	1.87E+00	5.36E-03
2.60E-09	2.61E+00	-6.37E-03
2.80E-09	2.77E+00	-1.69E-02
3.00E-09	2.91E+00	-1.11E-02
3.20E-09	3.54E+00	-1.94E-02
3.40E-09	4.29E+00	-4.67E-02
3.60E-09	4.70E+00	-7.78E-02
3.80E-09	4.88E+00	-5.59E-02
4.00E-09	5.04E+00	1.68E-01
4.20E-09	5.34E+00	7.30E-01
4.40E-09	5.90E+00	3.11E+00
4.60E-09	6.36E+00	9.14E+00
4.80E-09	6.38E+00	9.65E+00
5.00E-09	6.37E+00	9.91E+00
5.20E-09	6.72E+00	9.98E+00
5.40E-09	7.15E+00	9.98E+00
5.60E-09	7.35E+00	9.99E+00
5.80E-09	7.43E+00	9.99E+00
6.00E-09	7.47E+00	1.00E+01
6.20E-09	7.62E+00	1.00E+01
6.40E-09	7.93E+00	1.00E+01
6.60E-09	8.19E+00	9.99E+00
6.80E-09	8.19E+00	1.00E+01
7.00E-09	8.13E+00	1.00E+01
7.20E-09	8.30E+00	1.00E+01
7.40E-09	8.58E+00	1.00E+01
7.60E-09	8.69E+00	1.00E+01
7.80E-09	8.70E+00	9.99E+00
8.00E-09	8.73E+00	1.00E+01
8.20E-09	8.62E+00	9.99E+00
8.40E-09	8.24E+00	1.00E+01
8.60E-09	7.61E+00	9.99E+00
8.80E-09	6.89E+00	1.00E+01
9.00E-09	6.42E+00	1.00E+01
9.20E-09	6.31E+00	1.00E+01
9.40E-09	6.06E+00	1.00E+01
9.60E-09	5.42E+00	1.00E+01
9.80E-09	4.85E+00	1.00E+01
1.00E-08	4.62E+00	1.00E+01
1.02E-08	4.46E+00	1.00E+01
1.04E-08	4.23E+00	1.00E+01
1.06E-08	3.88E+00	1.00E+01
1.08E-08	3.43E+00	1.01E+01
1.10E-08	3.16E+00	1.01E+01
1.12E-08	3.14E+00	1.00E+01
1.14E-08	3.04E+00	9.48E+00
1.16E-08	2.68E+00	8.59E+00
1.18E-08	2.40E+00	6.25E+00
1.20E-08	2.56E+00	5.92E-01
1.22E-08	3.23E+00	2.44E-01
1.24E-08	4.12E+00	6.80E-02
1.26E-08	4.59E+00	7.67E-02
1.28E-08	4.49E+00	2.18E-01
1.30E-08	4.51E+00	4.60E-01
1.32E-08	5.20E+00	8.29E-01
1.34E-08	5.93E+00	2.80E+00
1.36E-08	6.10E+00	8.55E+00
1.38E-08	6.04E+00	9.71E+00
1.40E-08	6.18E+00	9.80E+00

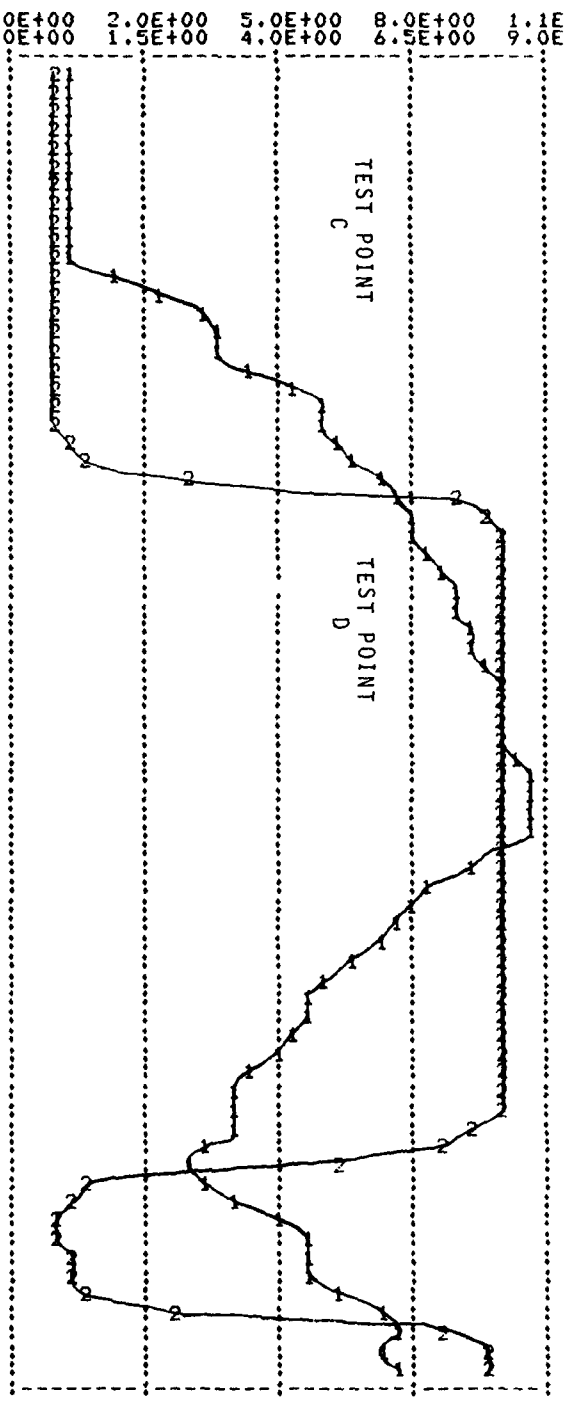


Figure 7-7 - CMOS/SOS Receiver Input/Output - Simple/Lumped

7.3.2 Microstrip - CMOS/SOS

For microstrip construction the power plane is located on the bottom of the substrate, resulting in a large separation between the power plane and the interconnect. As a result, the interconnect capacitance is reduced, and the characteristic impedance is increased. The coding for this configuration is given in Figure 7-8, and the computer plot of test points A and B of Figure 7-4 is given in Figure 7-9. Note that the driver output at point B does go to zero volts after switching from a logic one. The response of the device at the end of the interconnect is shown in Figure 7-10. These figures also show that the noise margin is normal. It is interesting to note that although this family operated marginally when simple/lumped interconnect were used, the family performs adequately when microstrip interconnects are used.

```
          F LIUS CKT
   LIUS        CKT          81/11/04.      15.38.04.
##  LIUS CKT##
E1 1 0 DC 10. TR PULSE(10.,0.,.2NS,1.NS,1.NS,5.NS,10.NS)
M1 2 0 1 3 RB9050A(25.)
E2 2 0 10.
R1 3 4 .05A
L1 4 5 7.4N
C1 5 0 .99P
R2 5 6 .05A
L2 6 7 7.4N
C2 7 0 .99P
R3 7 8 .05A
L3 8 9 7.4N
C3 9 0 .99P
R4 9 10 .05A
L4 10 11 7.4N
C4 11 0 .99P
M2 2 0 11 12 RB9020A(25.)

COM -  ? A LIUS TRAN
CONTROLS=? NOCONVERGE 150
CONTROLS=? SWEEP 1 FROM 0.NS TO 12.NS BY .1NS
CONTROLS=? SAVE V(1),V(3),V(11),V(12)
CONTROLS=? PLOT 1 34

ANALYSIS OF CIRCUIT LIUS UNDER ANALYSIS MODE TRAN
WITH THE FOLLOWING PARAMETERS SPECIFIED

NOCONVERGE     1.500000E+02

87 ITERATIONS WERE REQUIRED FOR THE FIRST POINT.
```

Figure 7-8 - Coding Microstrip - CMOS/SOS

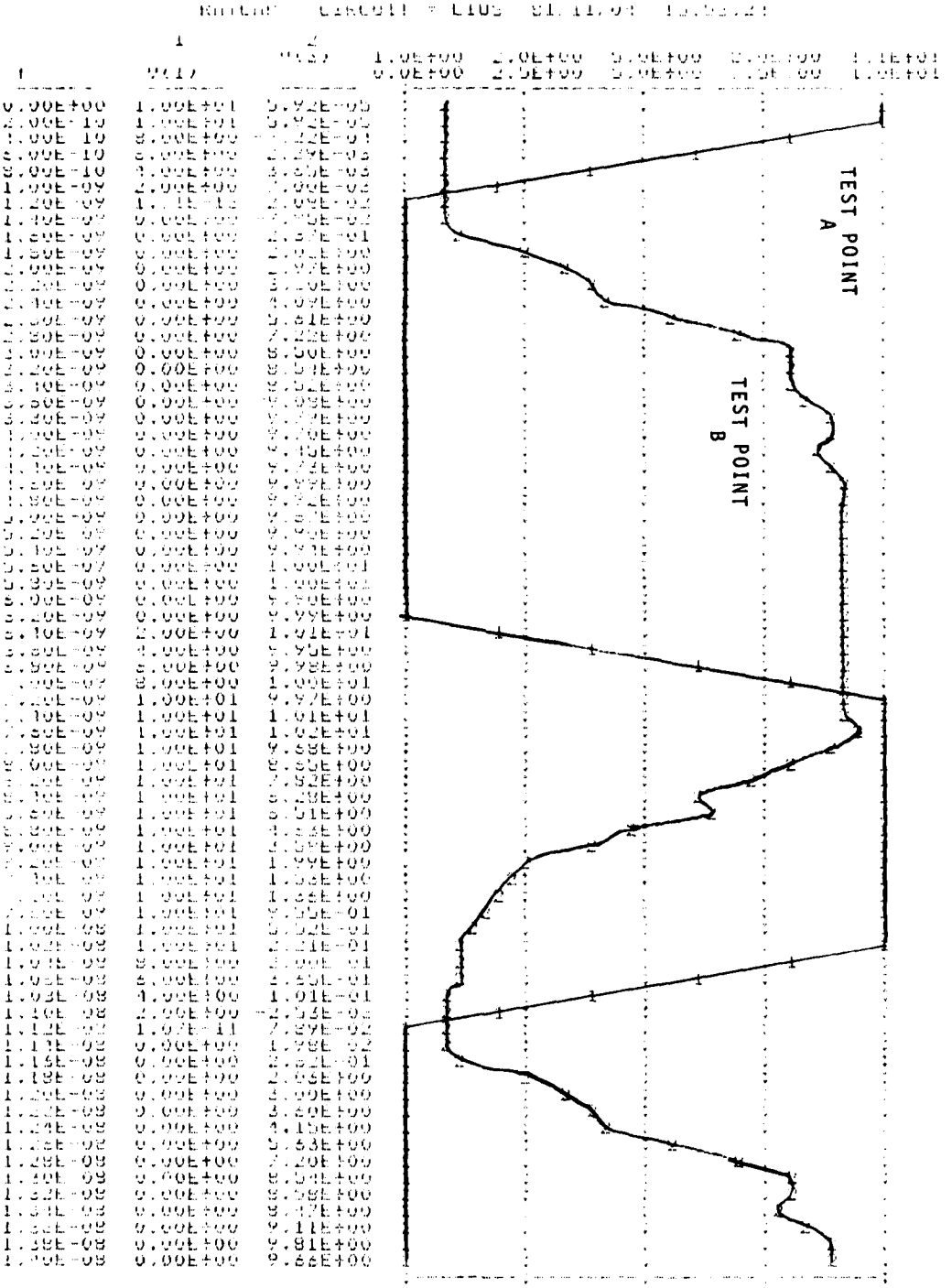


Figure 7-9 - CMOS/SOS Driver Input/Output - Microstrip

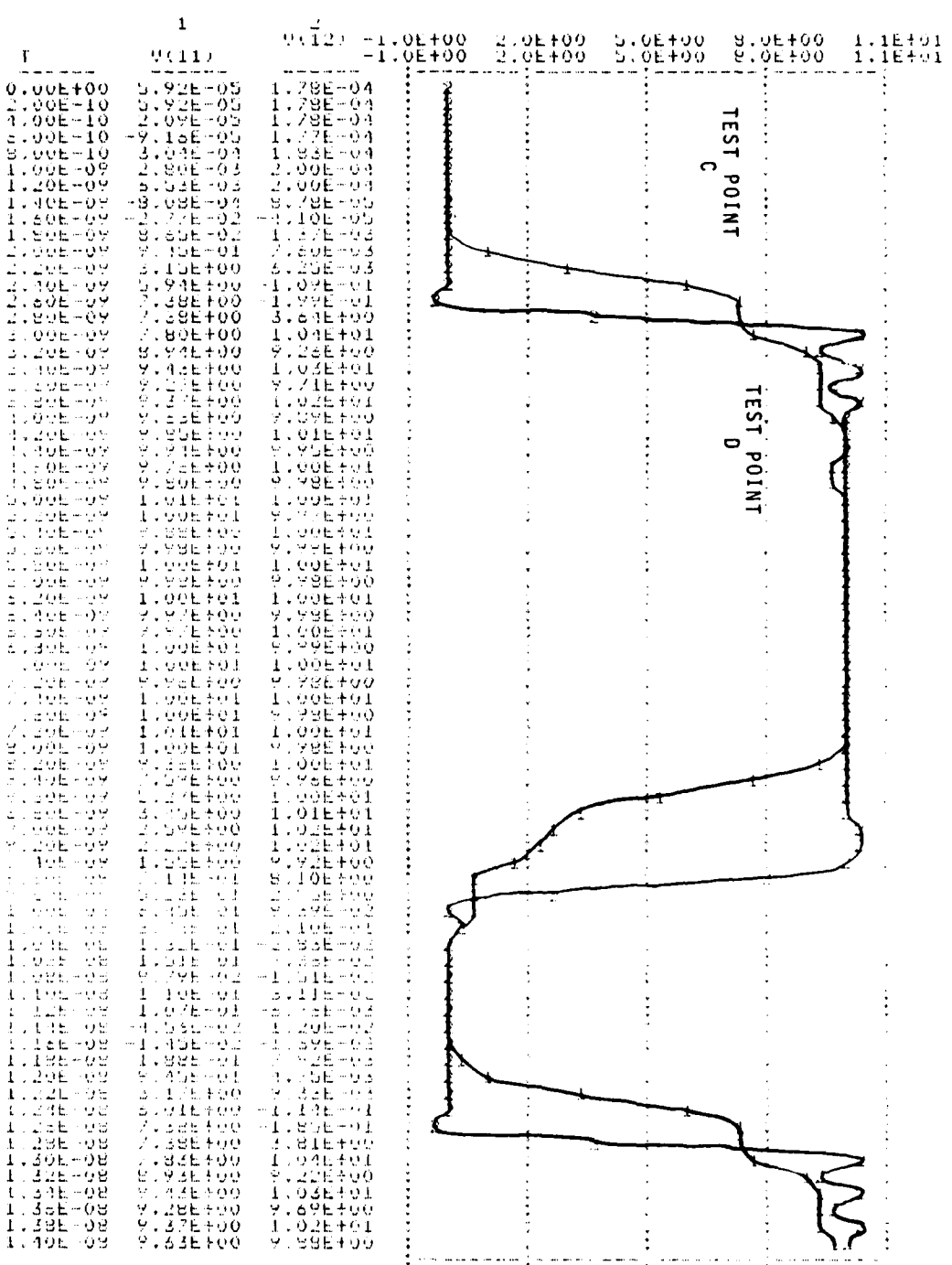


Figure 7-10 - CMOS/SOS Receiver Input/Output - Microstrip

8. FUNCTIONAL TEST HYBRIDS

The test circuit described in Section 6.2 will be implemented in five hybrid types. Four of these will contain four separate circuits, one for each selected family type. The fifth type, stripline, will contain a test circuit comprised of chip and wire 100K ECL devices. The other three logic families will not show improved performance using stripline construction.

The four types are:

- Simple/Lumped - HCC
- Simple/Lumped - Chip and Wire
- Microstrip - HCC
- Microstrip - Chip and Wire

8.1 Simple/Lumped - HCC

The simple/lumped version with HCCs shown in the photograph in Figure 8-1, has been fabricated and assembled. The test circuit for each logic family is comprised of three devices: At the very top of the figure is the 100K ECL family, followed by the STTL family. The third set of devices shown is the LSTTL family. At the bottom of the figure is the CMOS/SOS family. At appropriate locations test points that will accommodate the coaxial probe, described earlier, are incorporated. The following paragraphs describe the test results on the four family circuit types.

8.1.1 CMOS/SOS Family

Presently, initial testing performed on this family has shown that it has limited drive capability. The coaxial probe and coax cable with its associated capacitance slows down the CMOS/SOS outputs. Also, transmission line effects, due to the unterminated cable, can be observed on the waveform edges (see Figure 8-2). This difficulty is overcome when a FET probe, interfaced directly to the substrate, is used (see Figure 8-3).

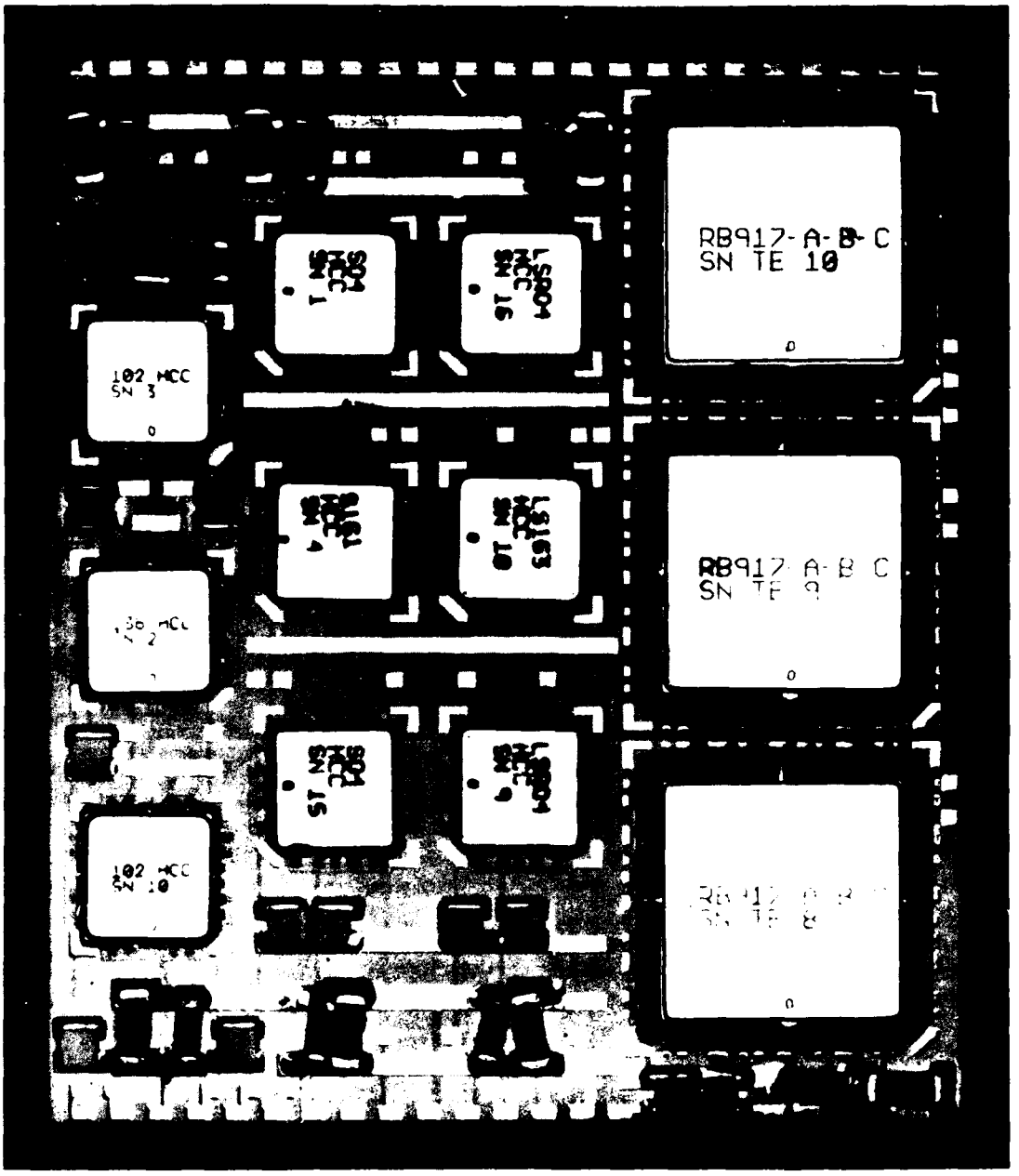


Figure 8-1 - Hybrid - Simple/Lumped HCC

CLOCK

DIVIDE
BY
2

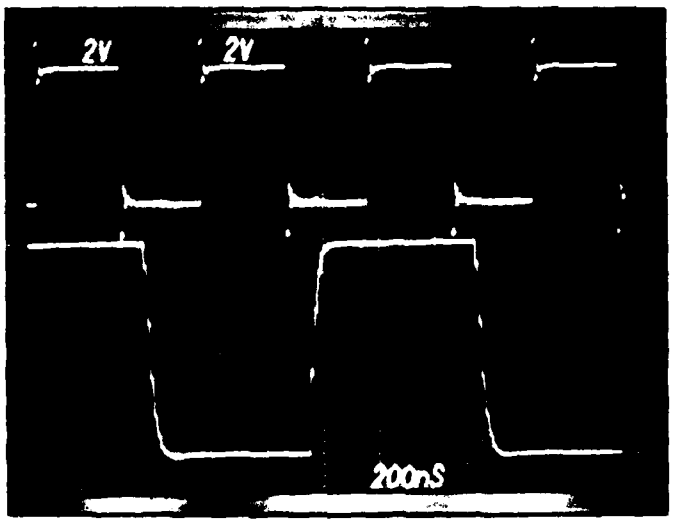


Figure 8-2 - CMOS/SOS Counter - COAX Probe

CLOCK

DIVIDE
BY
2

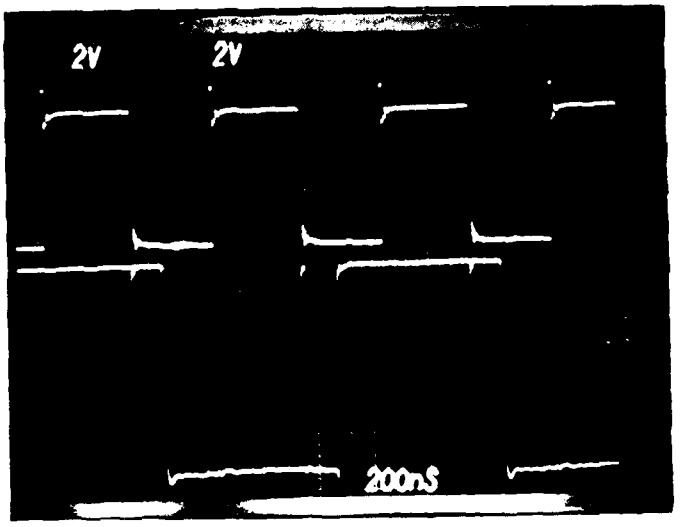


Figure 8-3 - CMOS/SOS Counter - FET Probe

The measured rise and fall time of this circuit was 7 to 8 nsec. The clock frequency to the counter was increased to the point where the counter stopped counting. This frequency was 23 MHz, which could be a result of the delays internal to the counter or the interconnect capacitance. Some insight as to the cause should be gained when the microstrip version is tested.

8.1.2 LSTTL Family

For most of these measurements the counter was clocked at 10 MHz. Figure 8-4 depicts the input and output of the clock buffer, the clock and the counter outputs are shown in Figure 8-5.

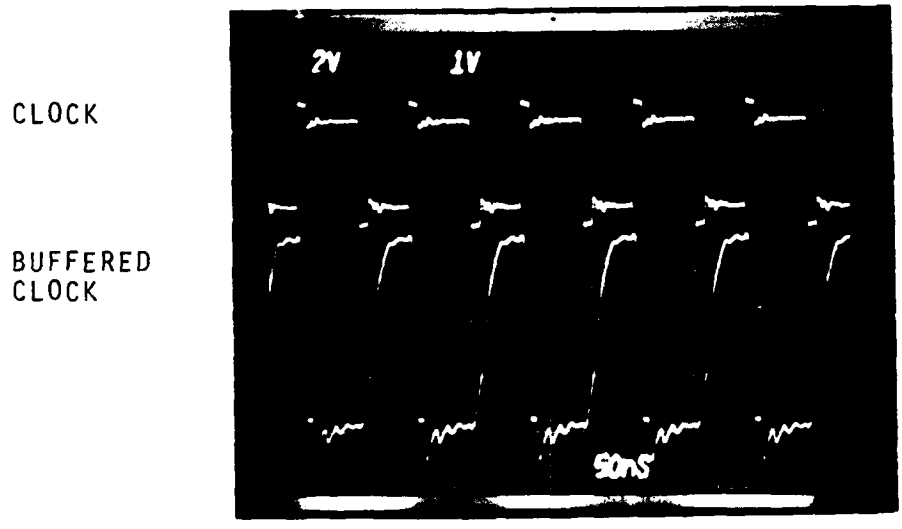


Figure 8-4 - LSTTL Buffered Clock

CLOCK

DIVIDE
BY
2

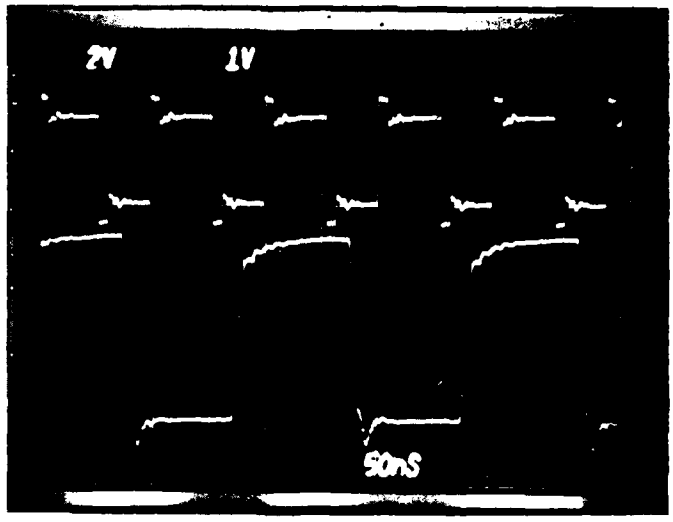


Figure 8-5 - LSTTL Counter Output

The average rise and fall times for the various outputs and the average propagation delay times were 10 nsec.

The counter is specified to clock typically at 25 MHz and at a maximum of 32 MHz. The actual frequency at which the counter stopped was 40 MHz. Here again until the microstrip version is tested, conclusions cannot be made. All the inputs and outputs were measured, and a scope photograph was taken. All of this data is contained in Appendix B1.

8.1.3 STTL Family

The testing was performed at 10 MHz. The clock and buffered clock are shown in Figure 8-6. When this figure is compared to Figure 8-4 of the LSTTL family, it is obvious that this family switches faster. Figure 8-7 depicts the clock and counter output. Because of the faster switching speeds more ringing is evident.

The average rise and fall times measured was 4 nsec. However, the average propagation delay time of 8 nsec was longer than expected. The counter, which is specified to operate at 70 MHz, could only be clocked to 50 MHz before dropping out. In this

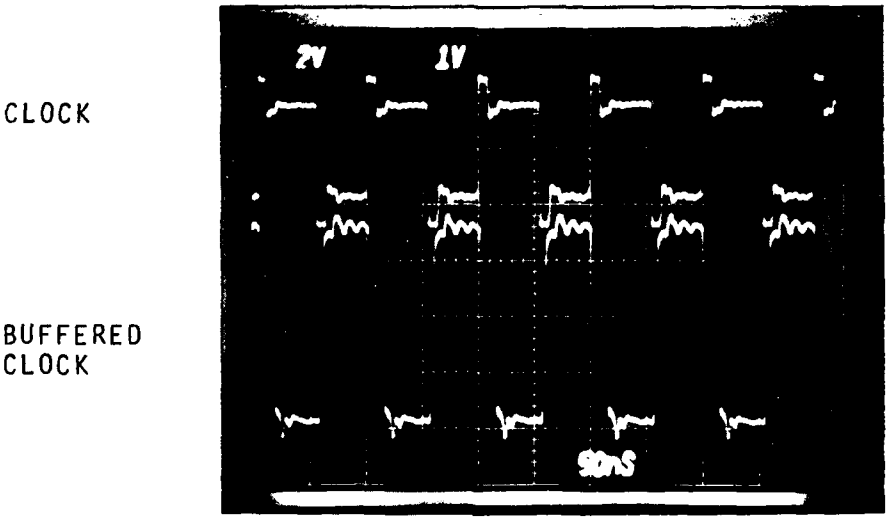


Figure 8-6 - STLL Buffered Clock

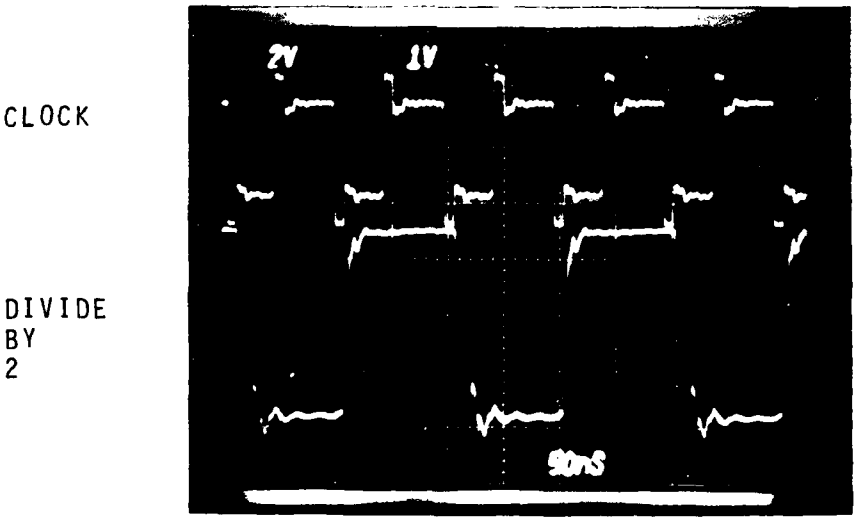


Figure 8-7 - STTL Counter Output

case, the counter frequency may have been limited by the interconnect capacitance. Data of all the outputs was recorded and is included as Appendix B2.

8.1.4 100K ECL Family

The 100K ECL family is specified to clock at rates up to 450 MHz. Presently the equipment available here can provide clocks up to 250 MHz, which should be adequate as this frequency meets the upper limit of the task requirement.

The fast edges inherent in these high frequencies can present measurement problems. These became apparent in the first set of measurements. To observe an output the coaxial probe was interfaced to a test point on the hybrid. A coaxial cable was used to connect the probe to a FET scope probe. When an output waveform was observed, it became apparent that transmission line effects were masking the performance of the logic. Looking at the input/output waveforms of the clock buffer, Figure 8-8, large amplitude ringing was observed. Ringing of this magnitude should false trigger the

CLOCK

BUFFERED CLOCK

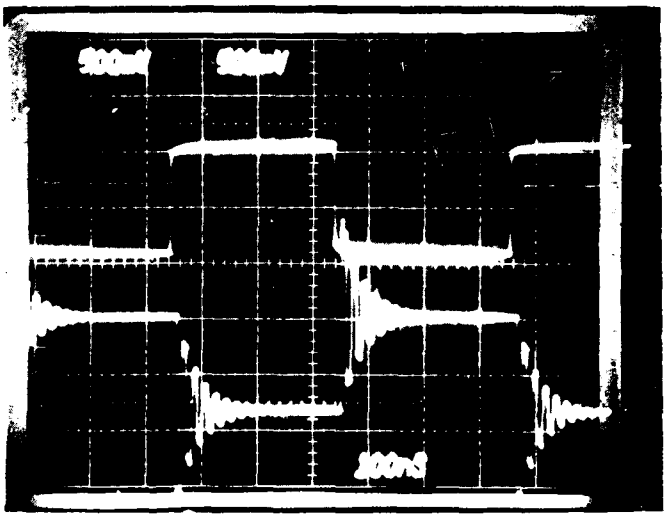


Figure 8-8 - 100K ECL Clock Buffer

counter. However, when the counter output was observed, the counter was operating properly (shown in Figure 8-9). This ringing was caused by the fast edges of the pulse reflecting from the unterminated coaxial cable.

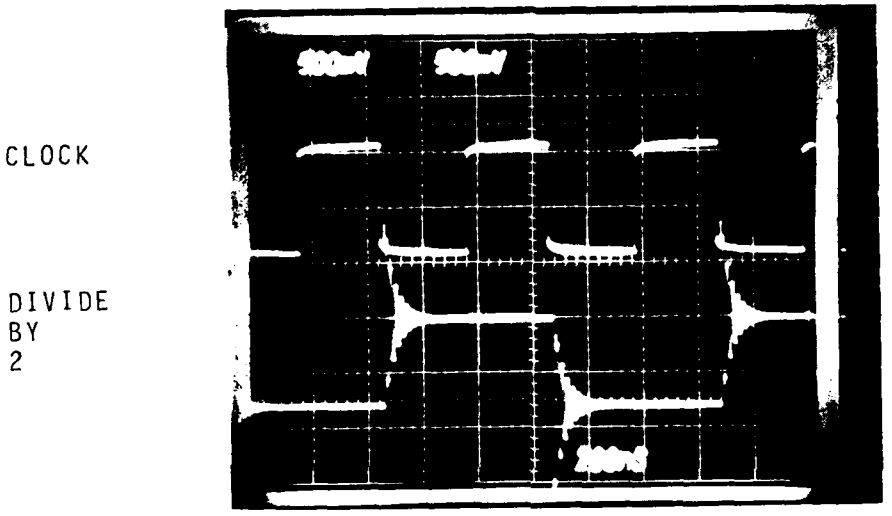


Figure 8-9 - 100K ECL Counter

Since 100K ECL has a high drive capability, the coaxial cable was connected directly to the 50 ohm scope input, terminating the cable and eliminating the ringing (see Figure 8-10 and 8-11).

The measured rise and fall times for this family was 1.5 nsec. Since the measurement is bandwidth limited by the scope, these switching times should be less than a nanosecond. The average propagation delay time measured was also 1.5 nsec.

The clock frequency to the counter was increased to discover the frequency at which counter would drop out. The counter was still operating when the upper limit of the pulse generator, 250 MHz, was reached. The clock and counter outputs are shown in

CLOCK

BUFFERED
CLOCK

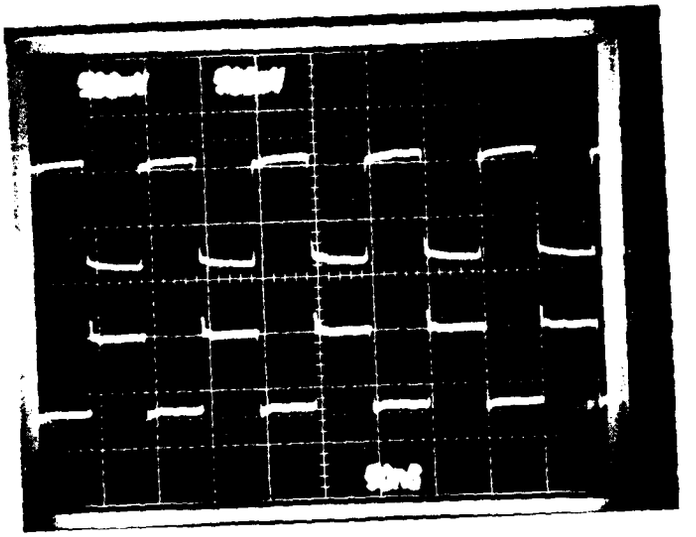


Figure 8-10 - 100K ECL Clock Buffer

CLOCK

DIVIDE
BY
2

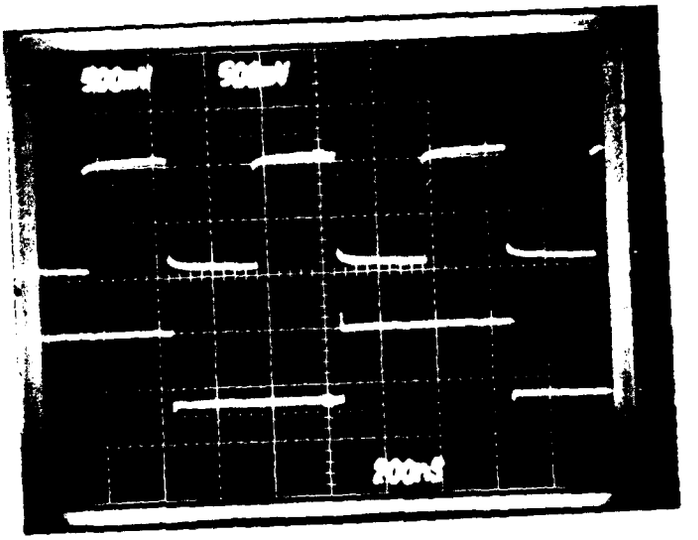


Figure 8-11 - 100K ECL Counter

Figure 8-12. Note that the waveforms are sinusoidal in nature. Because of the limited bandwidth of the measurement, the pulse could appear sinusoidal. The remainder of the test data are contained in Appendix B3.

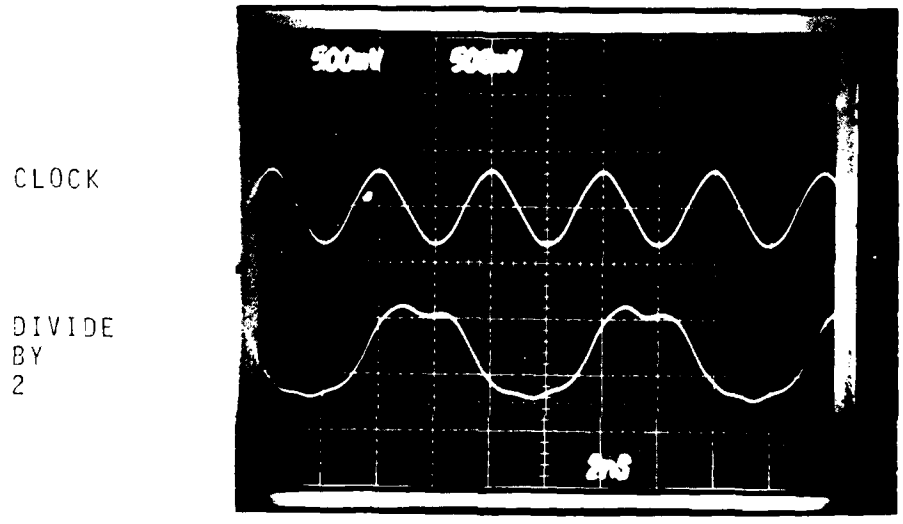


Figure 8-12 - 100K ECL Counter - 250 MHz

8.2 Other Test Hybrids

The simple/lumped chip and wire, microstrip chip and wire and microstrip HCC test hybrids have been fabricated and assembled. Photographs of these hybrids are contained in Figures 8-13, 8-14, and 8-15. These hybrids will all be tested in the near future.

The last hybrid type, stripline, is presently being fabricated. That too should be ready for assembly in the very near future. The layout of this version is shown in Figure 8-16.

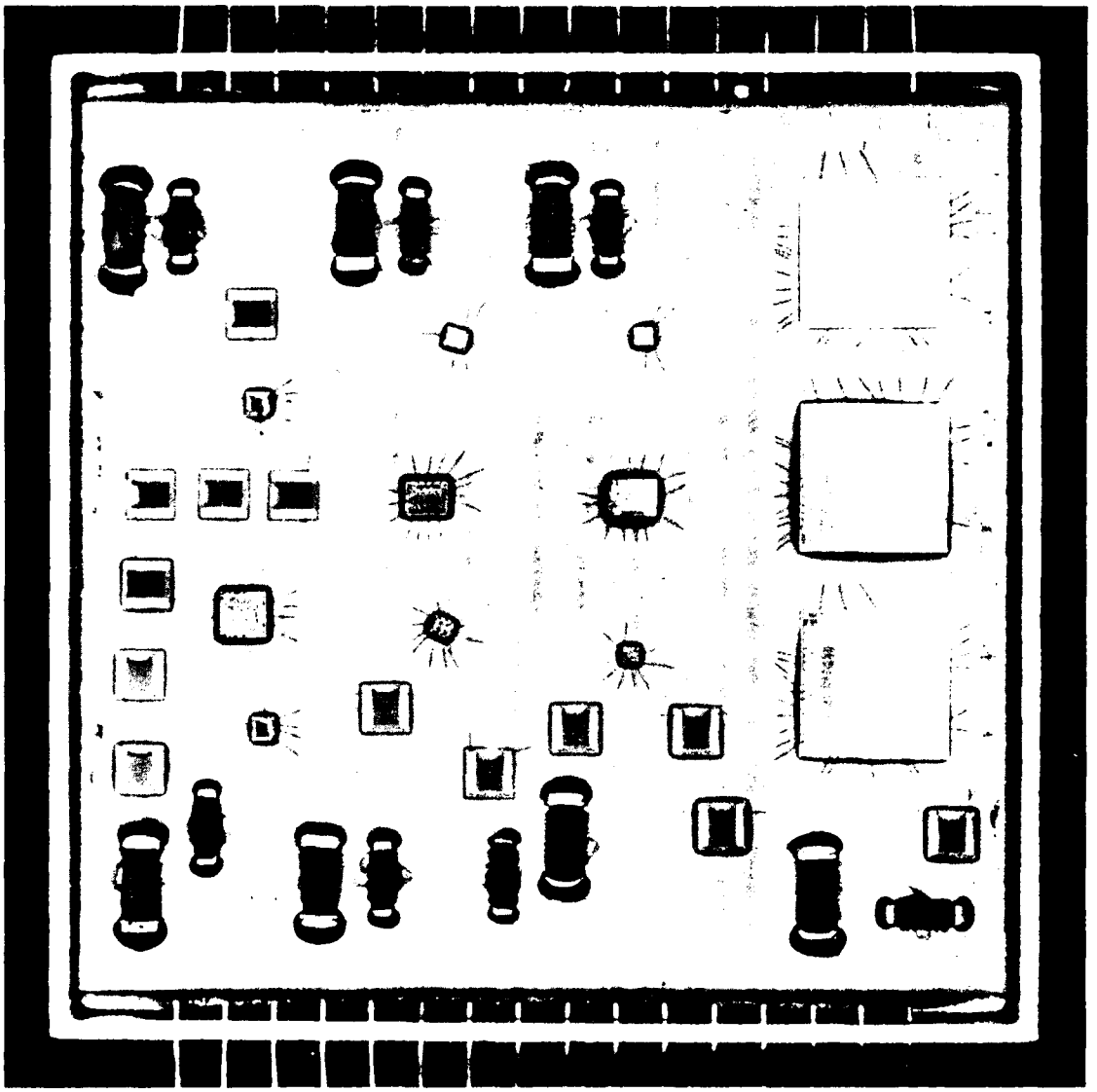


Figure 8-13 - Simple/Lumped Chip and Wire

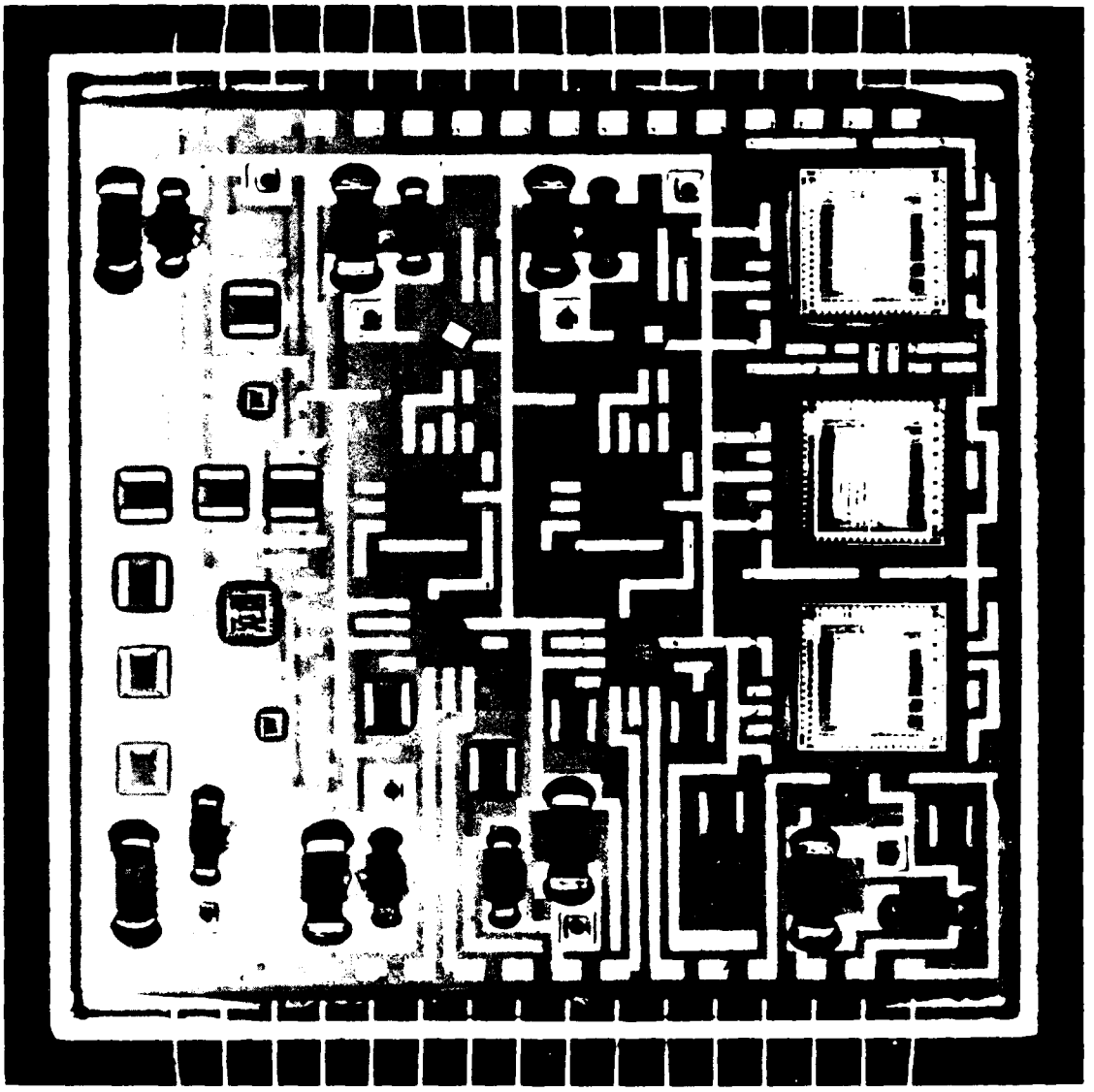


Figure 8-14 - Microstrip - Chip and Wire

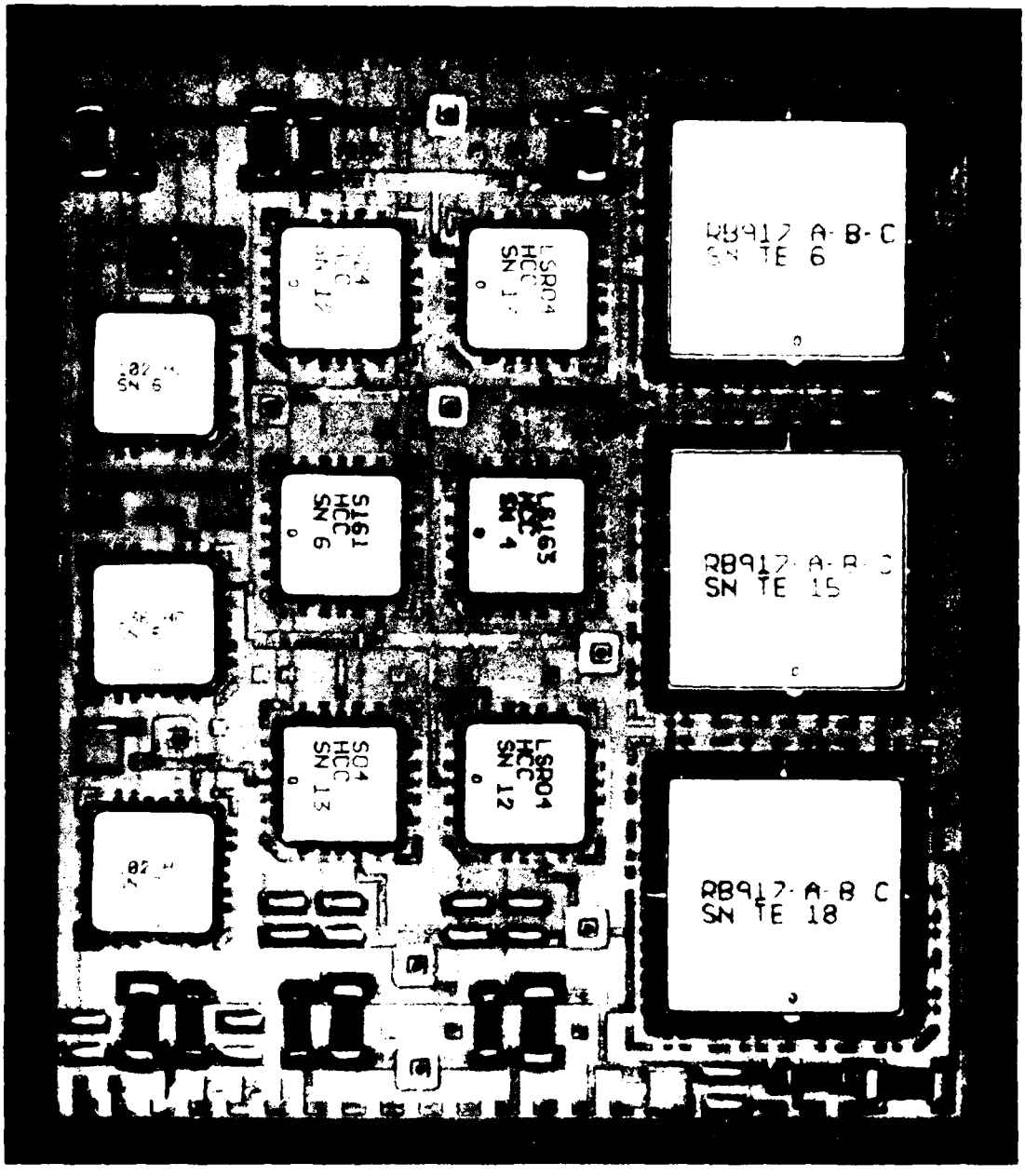


Figure 8-15 - Microstrip - HCC

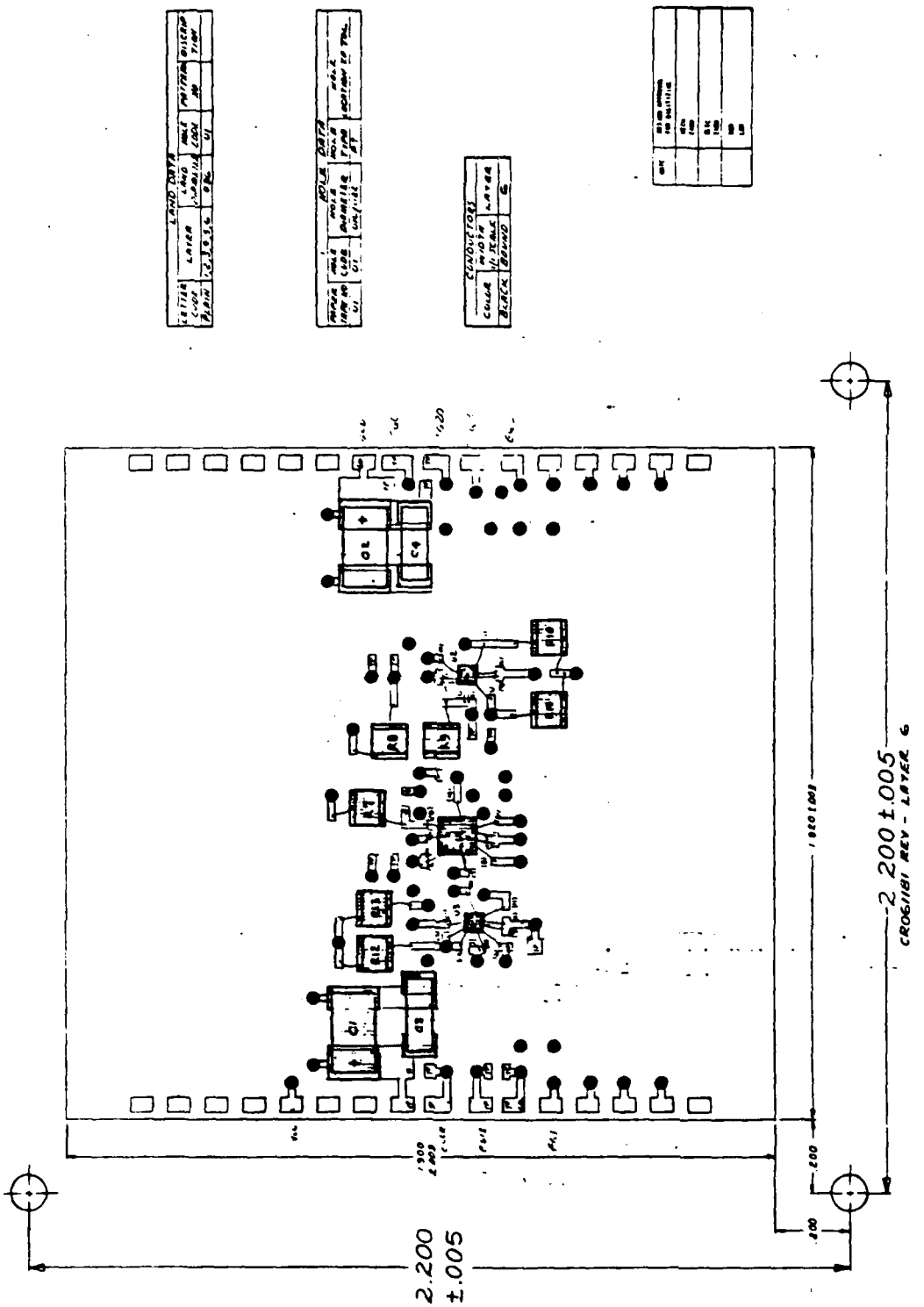


Figure 8-16 - Printed Wiring Board ECL Stripline

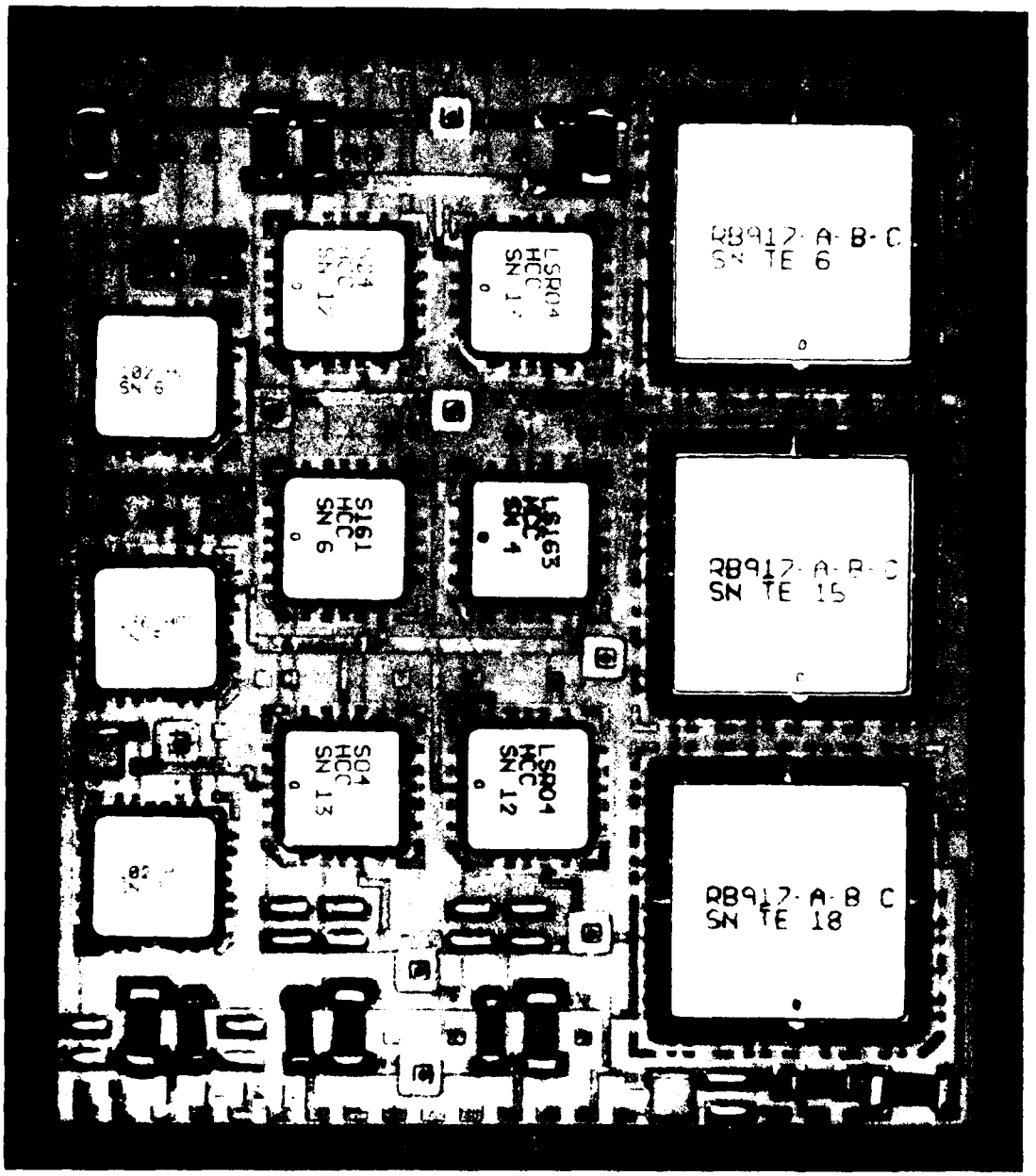


Figure 8-15 - Microstrip - HCC

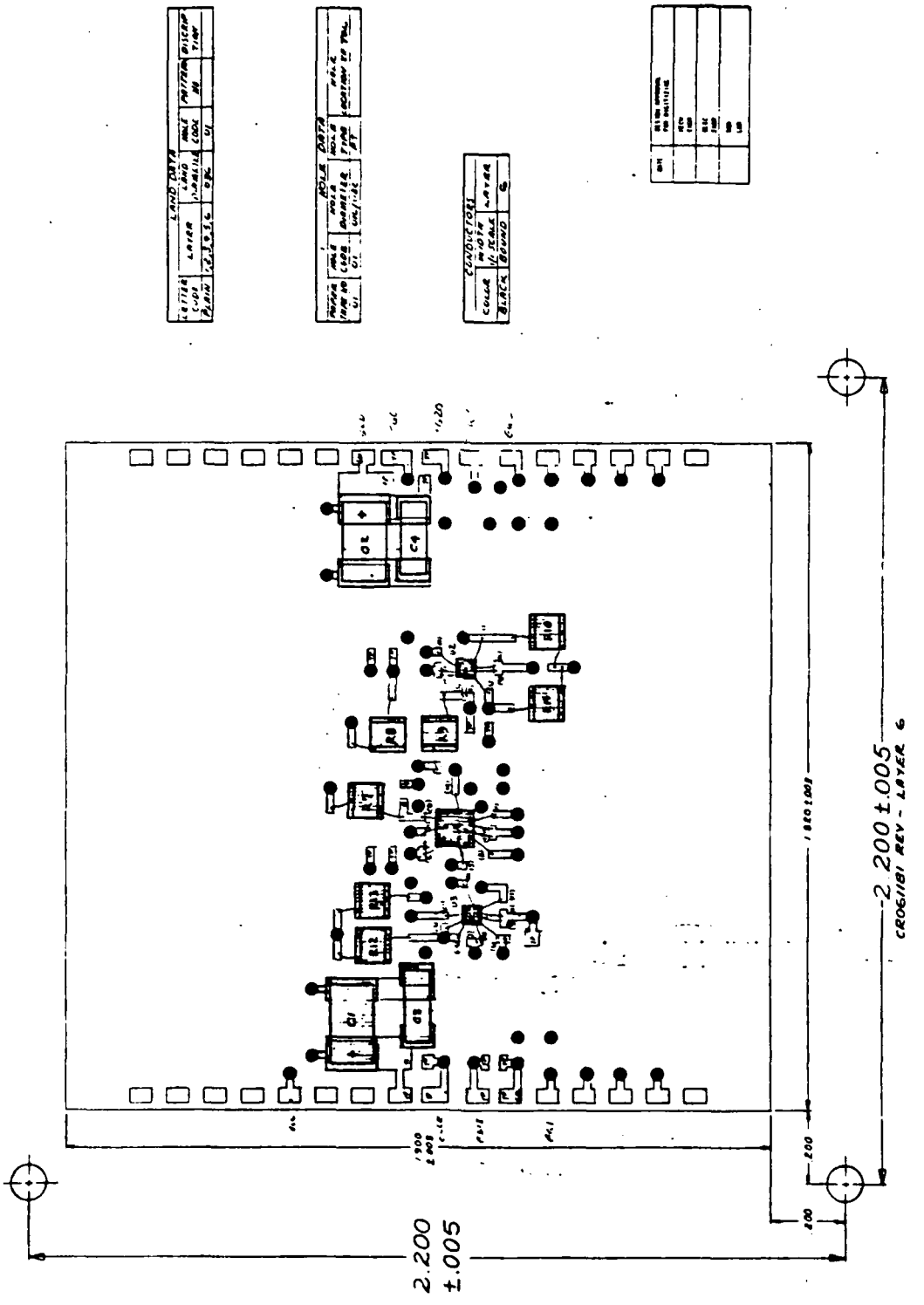


Figure 8-16 - Printed Wiring Board ECL Stripline

8.3 Initial CAD Guidelines

Not enough test data have been taken to establish the guidelines. However, some general comments can be made.

There will be a set of guidelines for each condition and for each logic family. For example there will be a set of guidelines for STTL logic and simple/lumped construction. If the construction is changed to microstrip then the guidelines will change.

The specific guidelines will be kept simple. This is to allow the incorporation of these guidelines into a CAD interconnect program. The conditions and specific guidelines are listed below:

1) Conditions

a) Construction

- Simple/Lumped
- Microstrip
- Stripline

b) Material

- 40 Mil Thick Ceramic
- 10 Mil Thick Polyimide

c) Line Width

- 10 Mil

d) Logic Families

- LSTTL
- STTL
- CMOS/SOS
- ECL

2) Specific Guidelines

a) Maximum Length

- Light Load
- Heavy Load
- 10 Branches

b) Minimum Separation

- Parallel Lines
- Alternate Layers

c) Maximum Crossovers

9. TASKS TO BE COMPLETED

The following is a list of the remaining tasks:

- Complete the evaluation of the test hybrids
- Generate initial guidelines for CAD hybrid interconnections
- Relayout the test circuits using the guidelines
- Purchase parts
- Fabricate and assemble test hybrids
- Evaluate hybrids
- Revise guidelines
- Second Interim Report
- Write Final Report

10. REFERENCES

(1) MECL System Design Handbook - W. Blood - Motorola Semiconductor Products - 12/72.

(2) High-Density High-Impedance Hybrid Circuit Technology for Gigahertz Logic - E. Lewis - IEEE Transactions on Components, Hybrid, and Manufacturing Technology - 12/79.

(3) W. R. Rohsenow, H.Y. Choi, **Heat Mass and Momentum Transfer**, Equation 8.35, Pgs 192 and 196, Prentice-Hall Inc., 1961, Third Printing, October 1965.

(4) W. R. Rohsenow, Op. Cit., Figure 8.11, Pg. 195.

(5) W. M. Kays, A. L. London, **Compact Heat Exchangers**, Figure 7-4, Pg. 126, McGraw-Hill Book Co., 1964, Second Edition.

(6) W. M. Kays, Op. Cit., Figure 10-26, Pg. 195.

(7) Raytheon Memo No. EAM:78:037, **High Speed Digital Packaging Proposal Thermal Management**, dtd 23 January 1978.

(8) Raytheon Report BR-10238-1, **Proposal for High Speed Digital Packaging, Volume 1 - Technical**, dtd 1 February 1978, Table 4-9 Pg. 4-74.

APPENDIX A

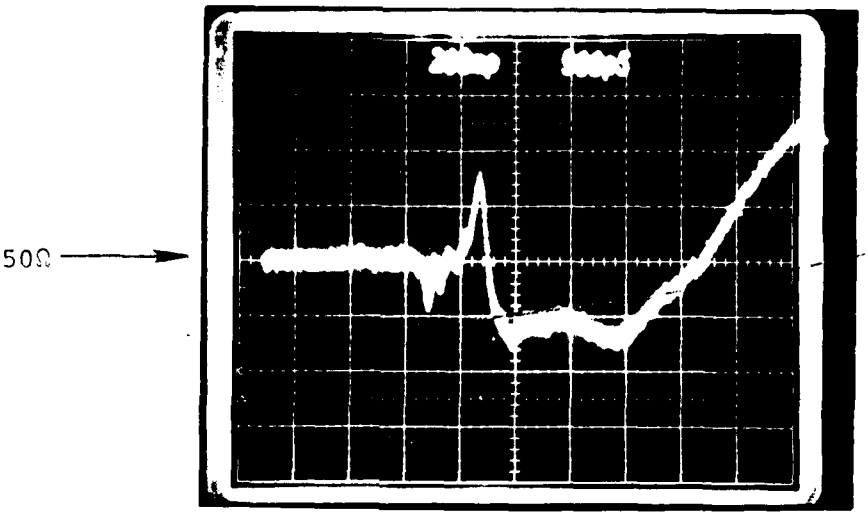


Figure A1 - Line 3

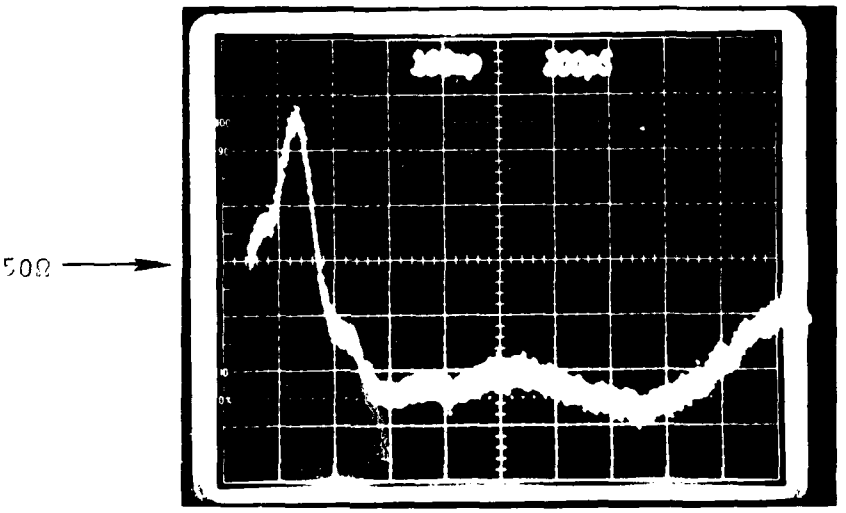


Figure A2 - Line 3

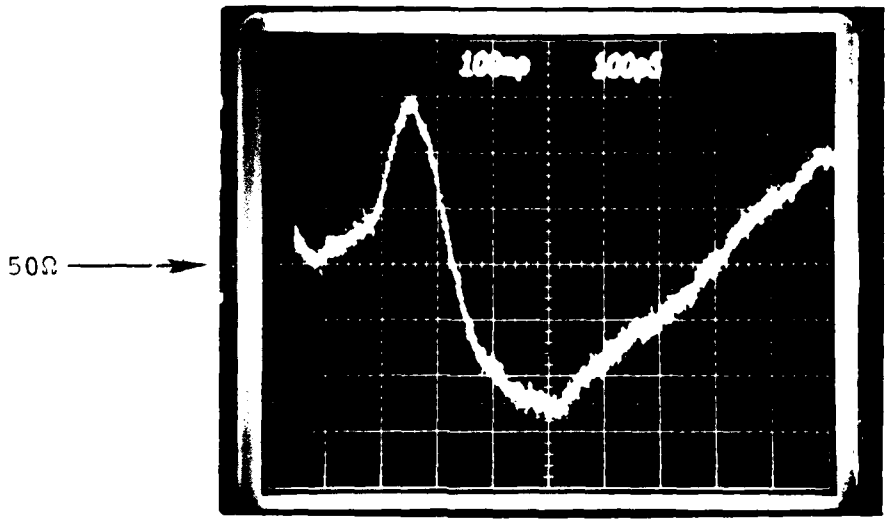
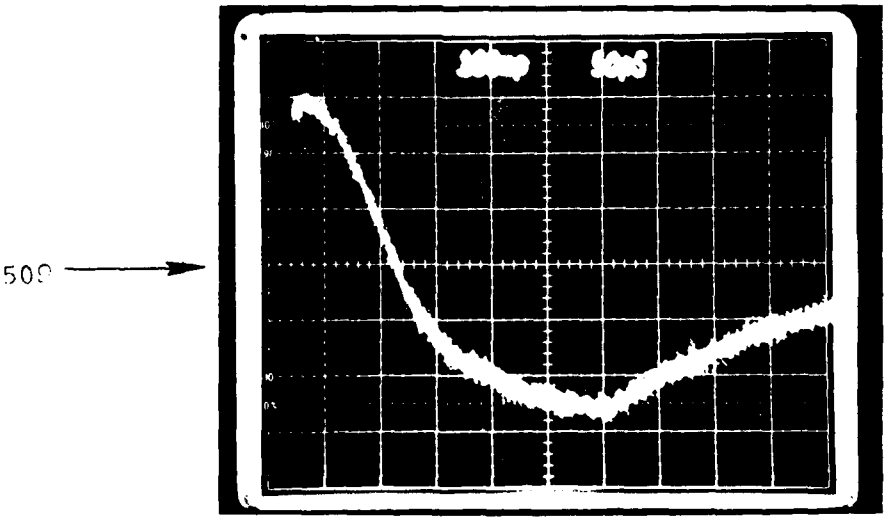


Figure A3 - Line 4



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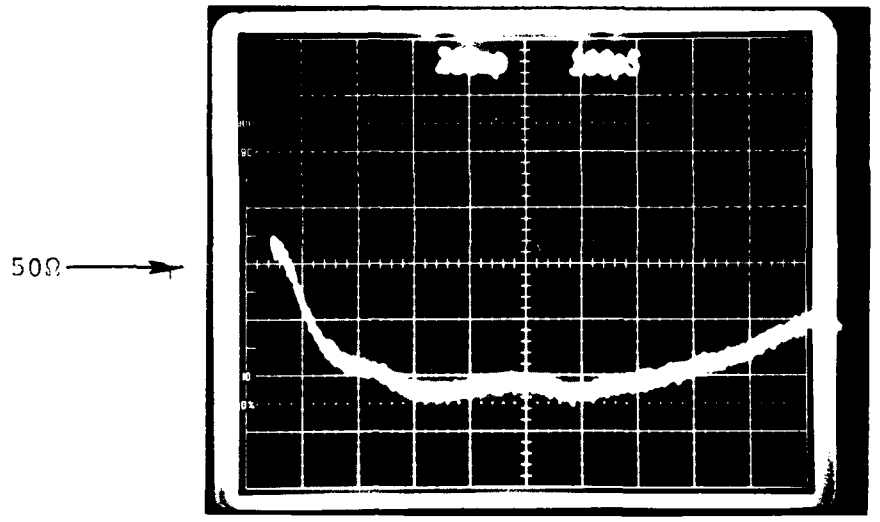

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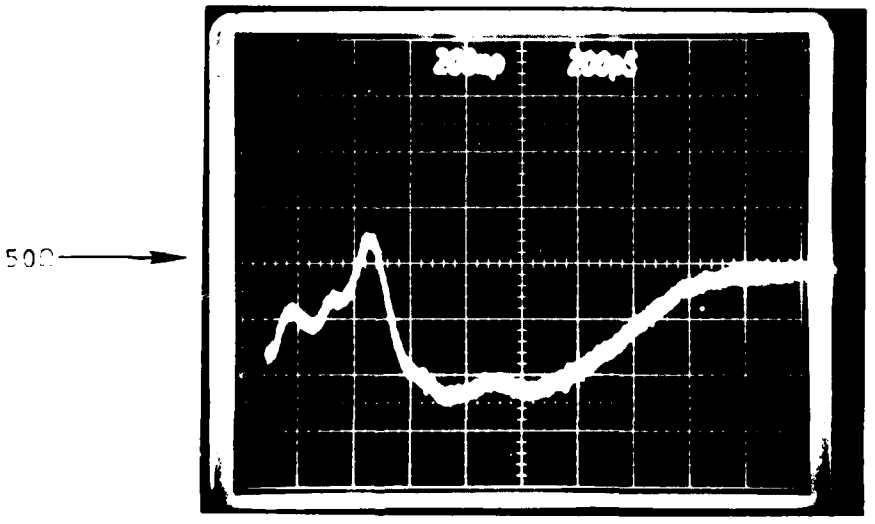

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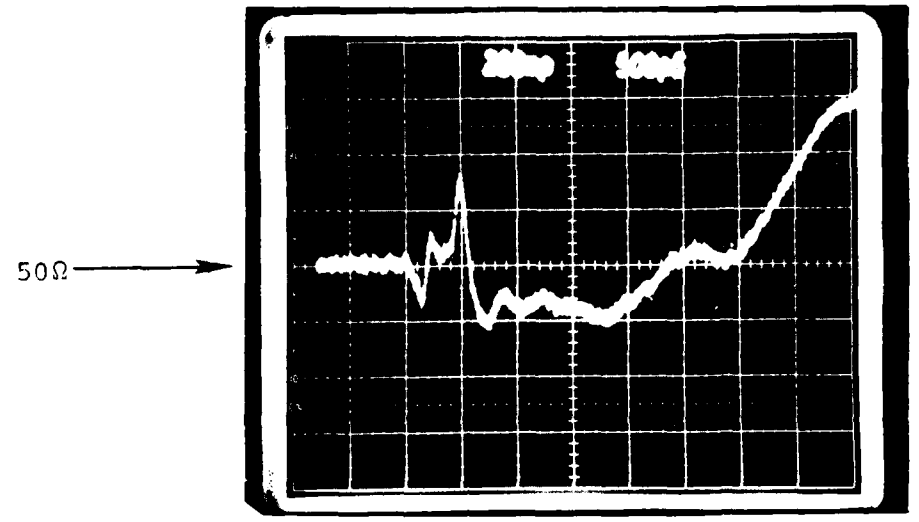

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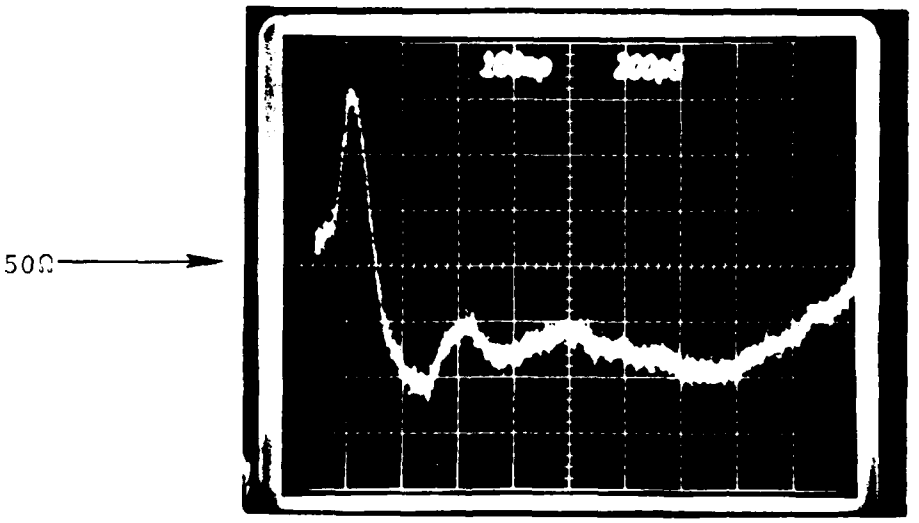

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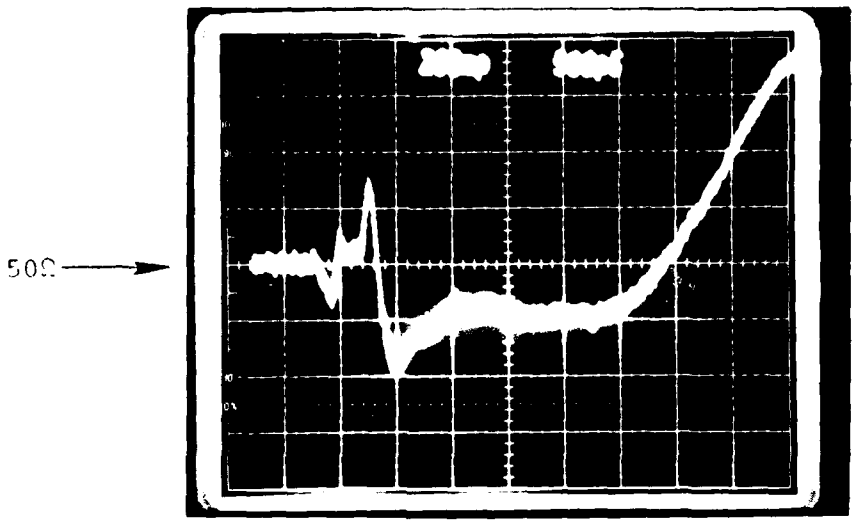

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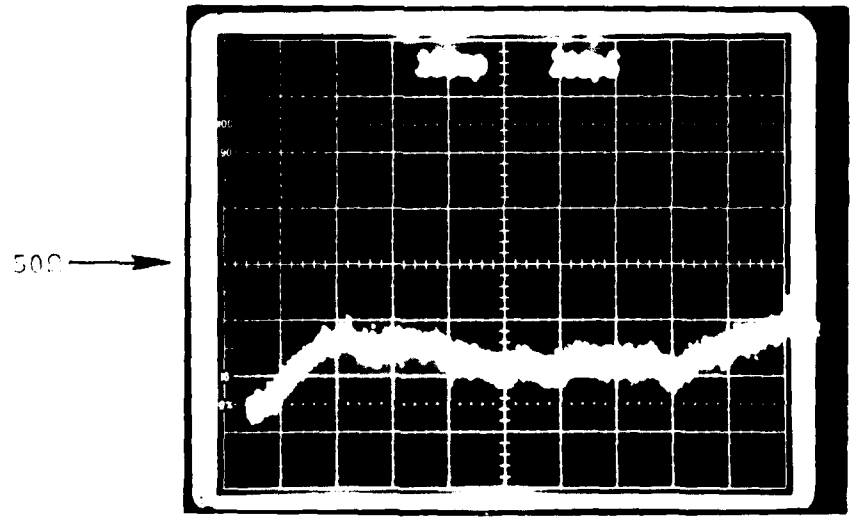

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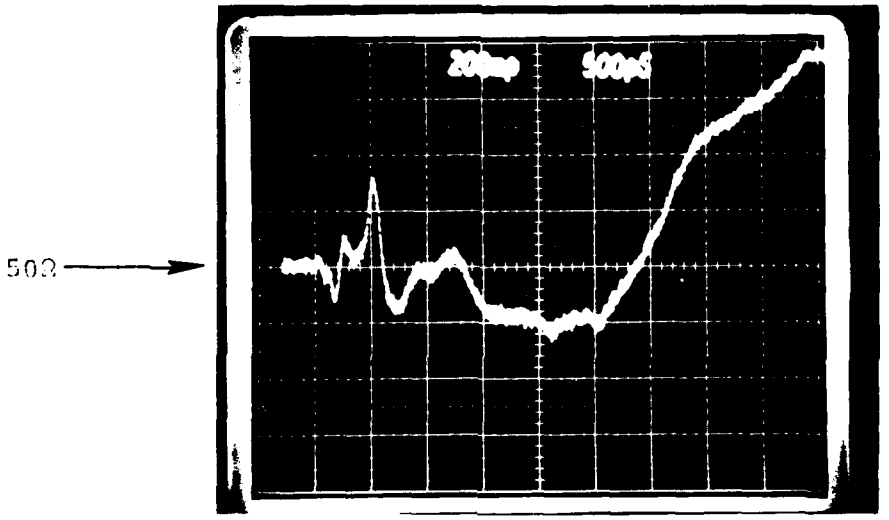

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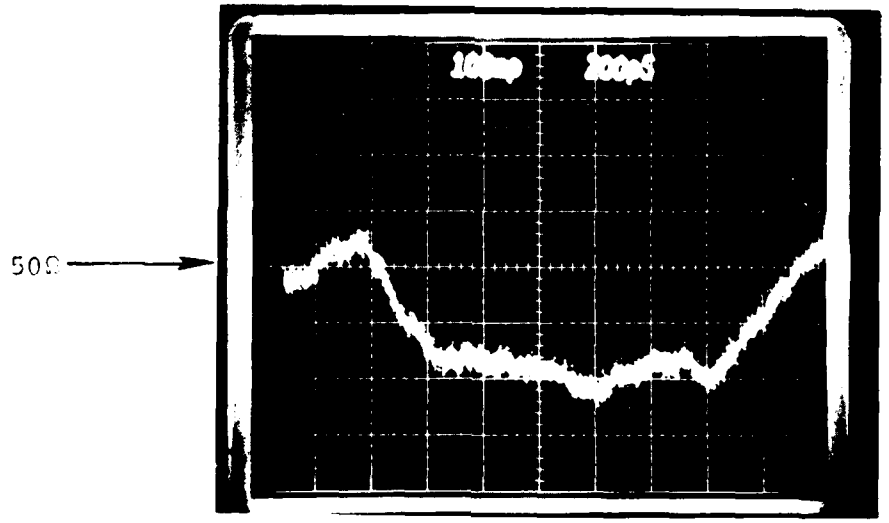

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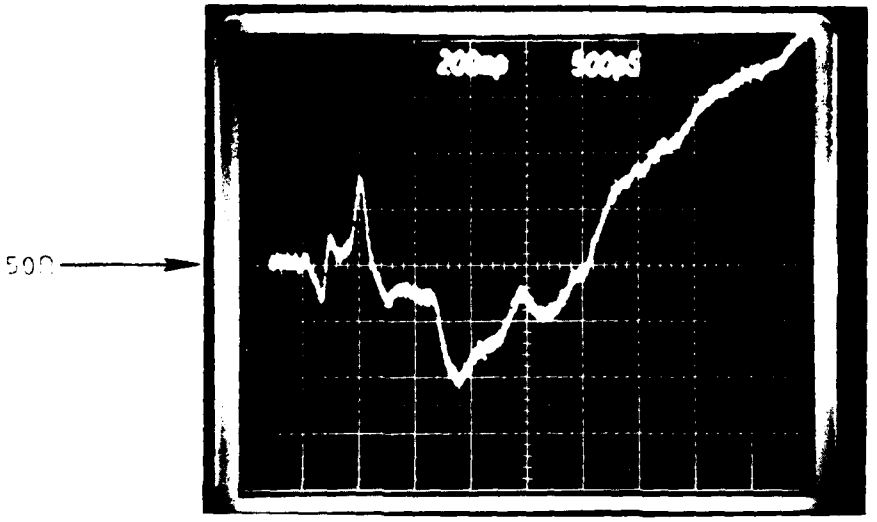

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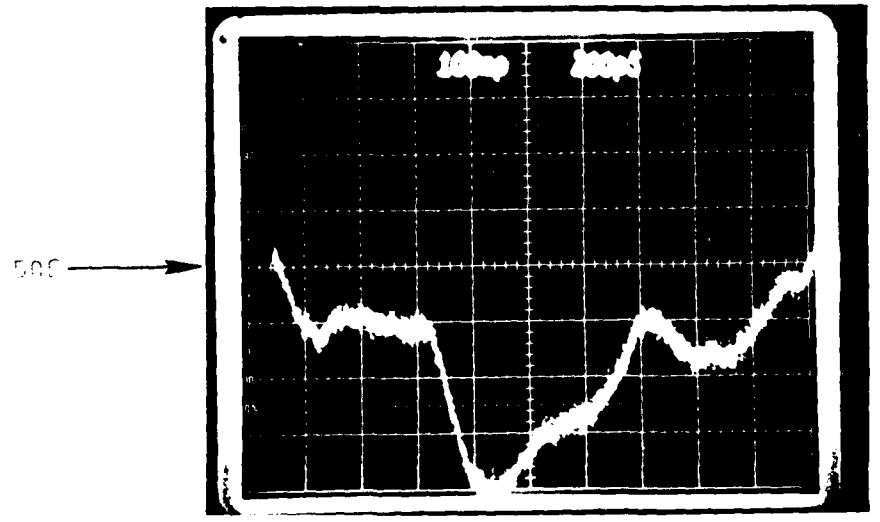

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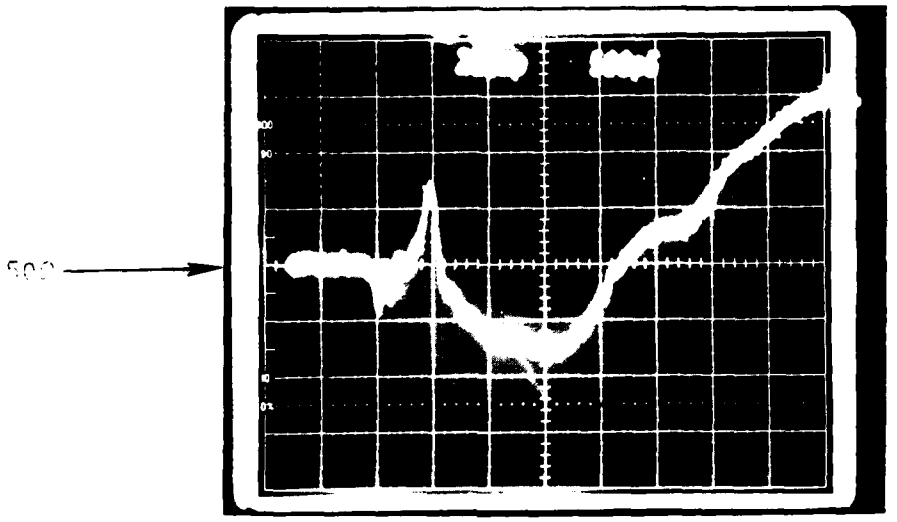

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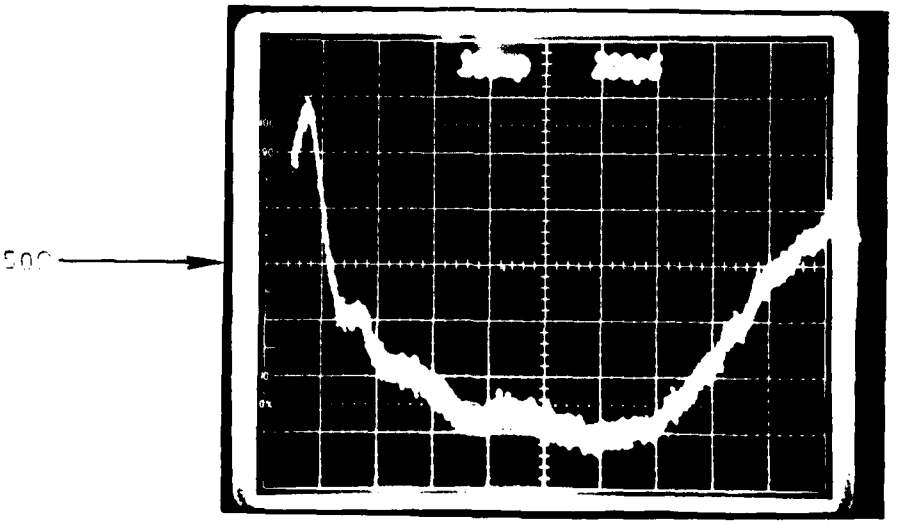

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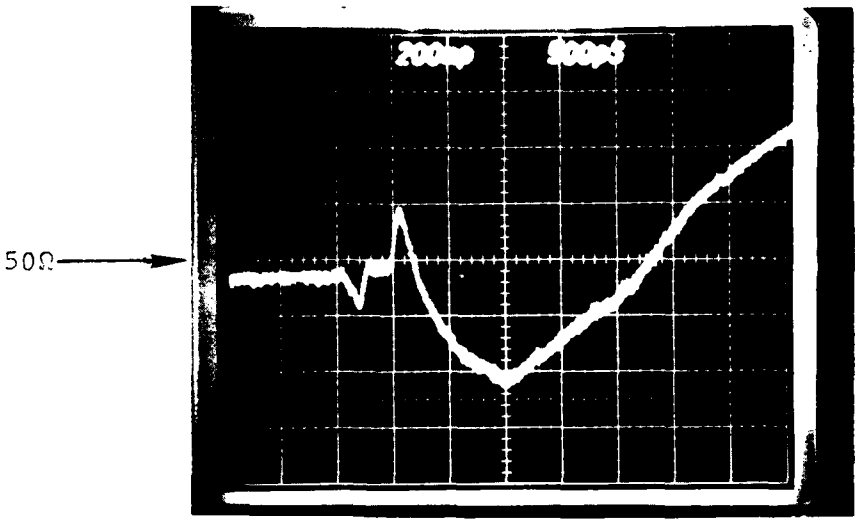

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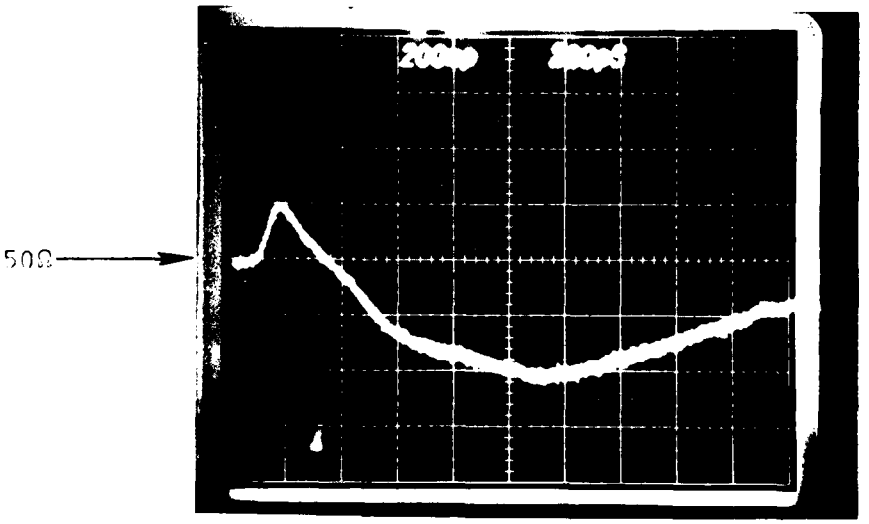

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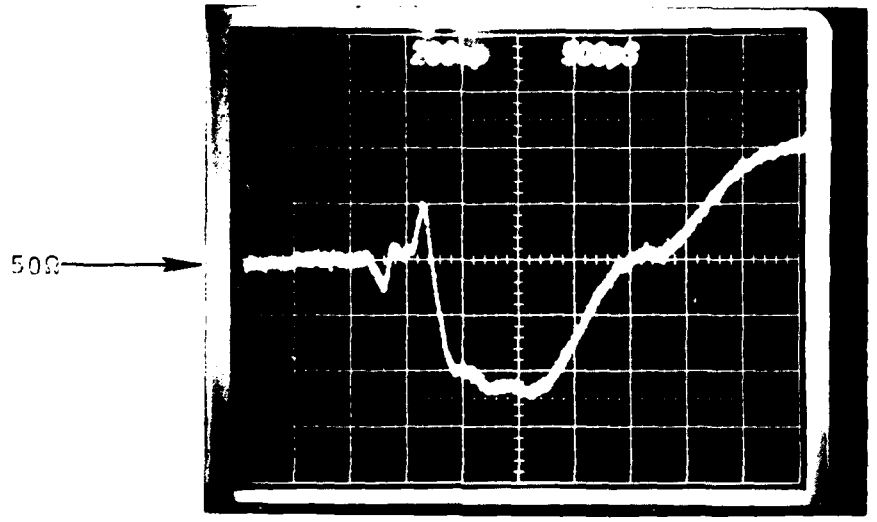

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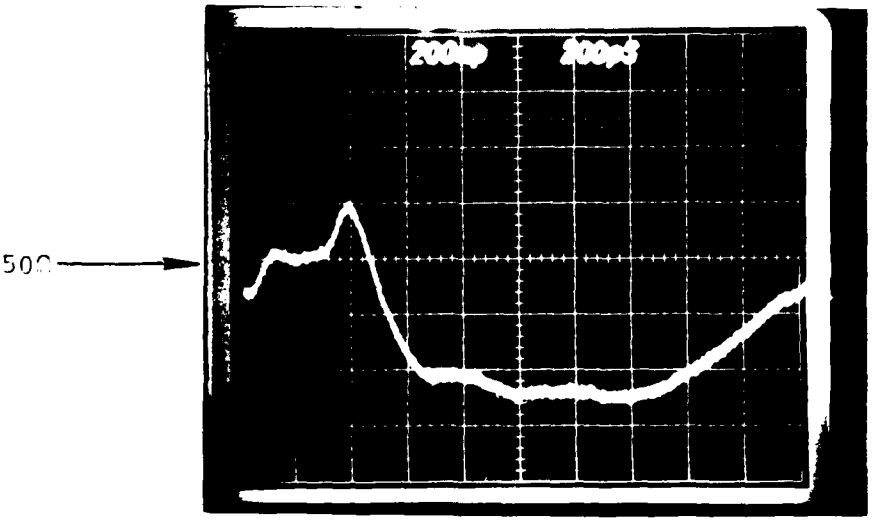

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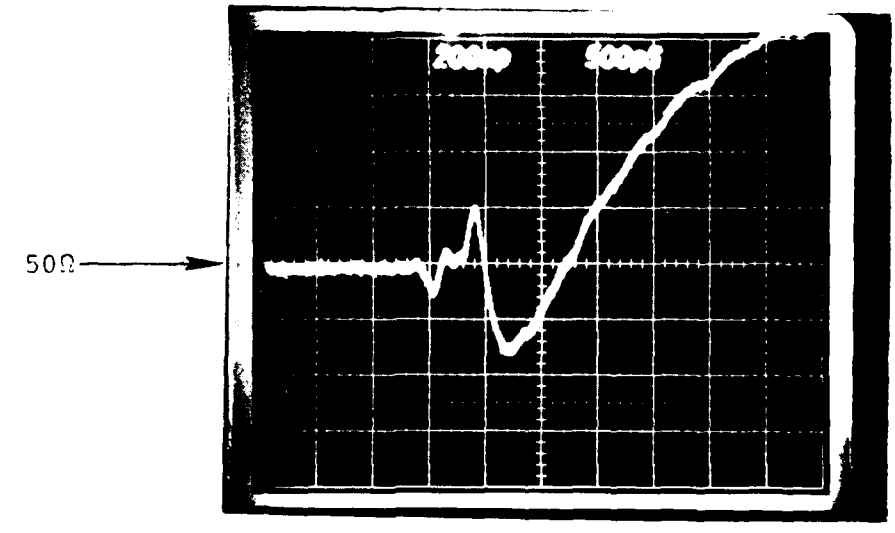

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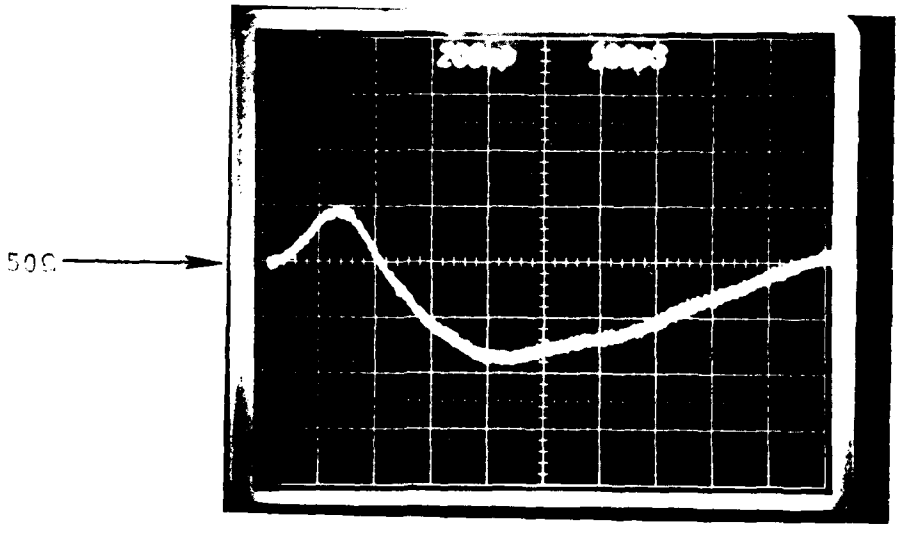

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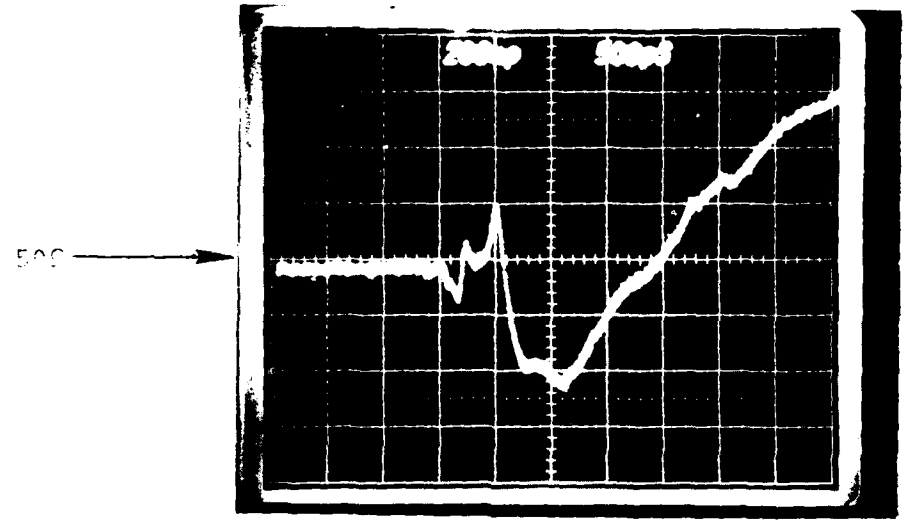

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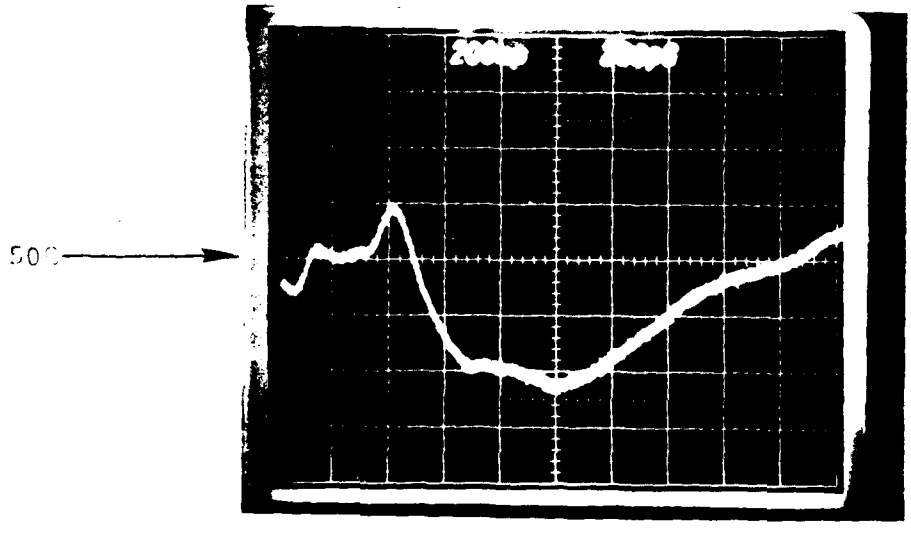

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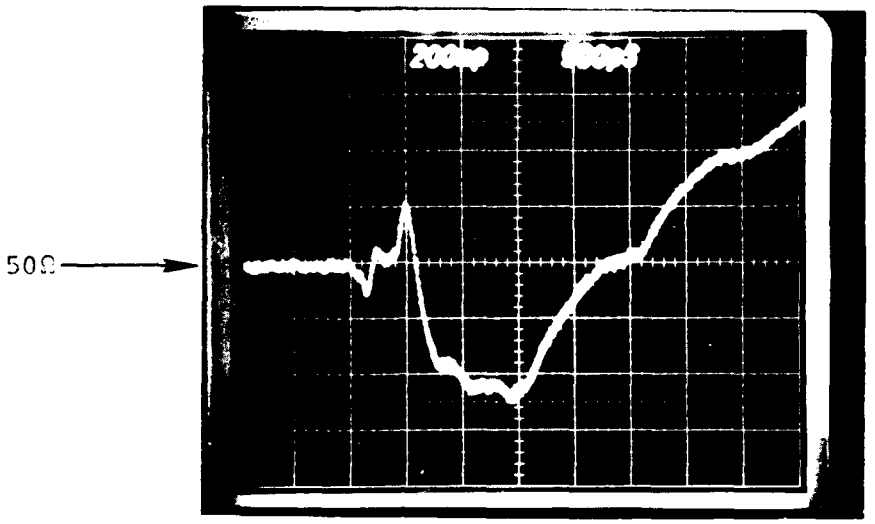

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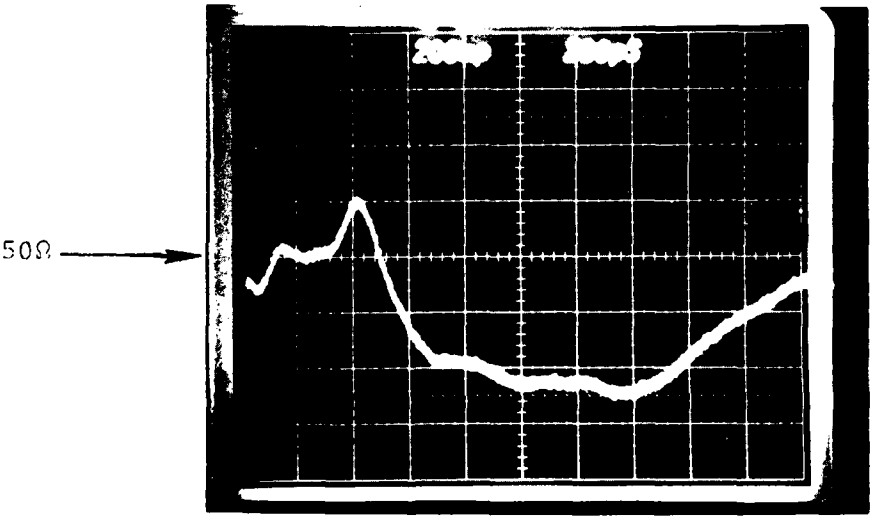

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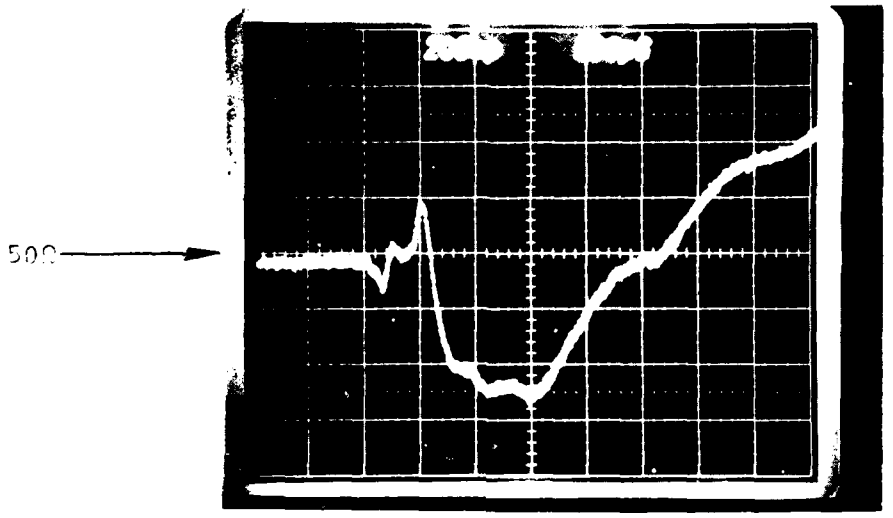

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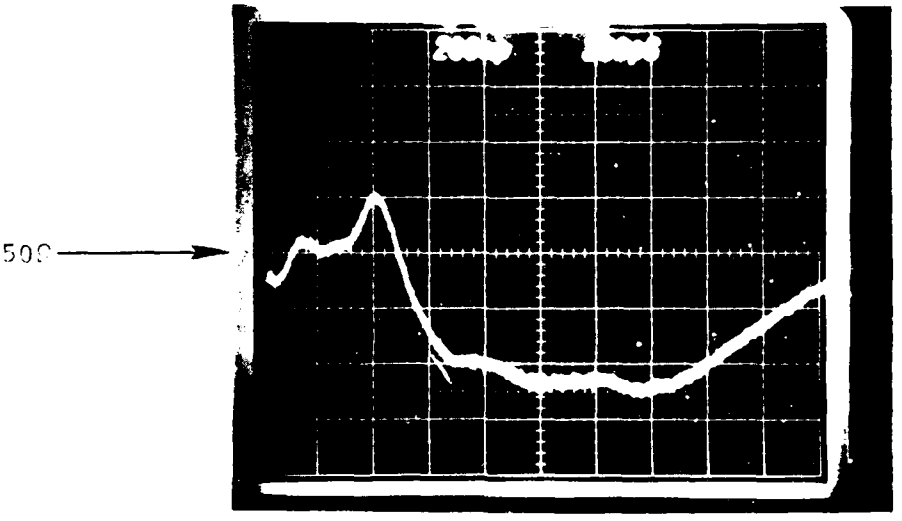

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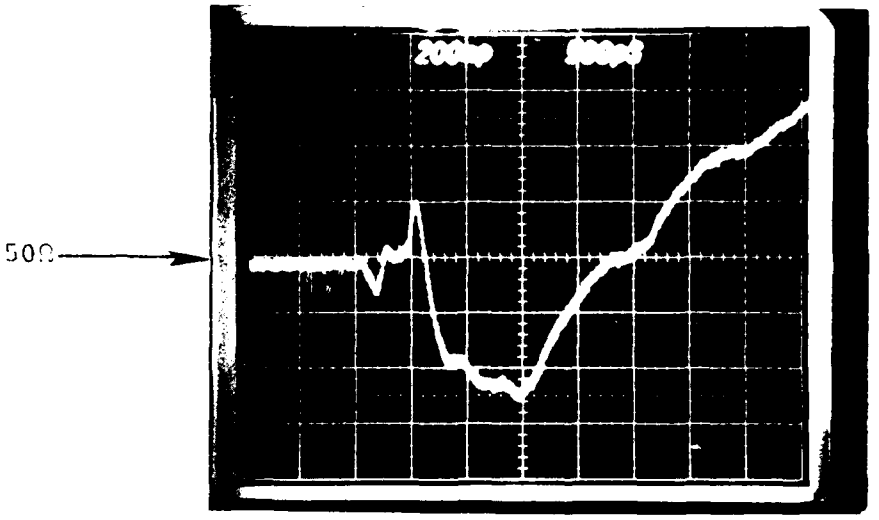

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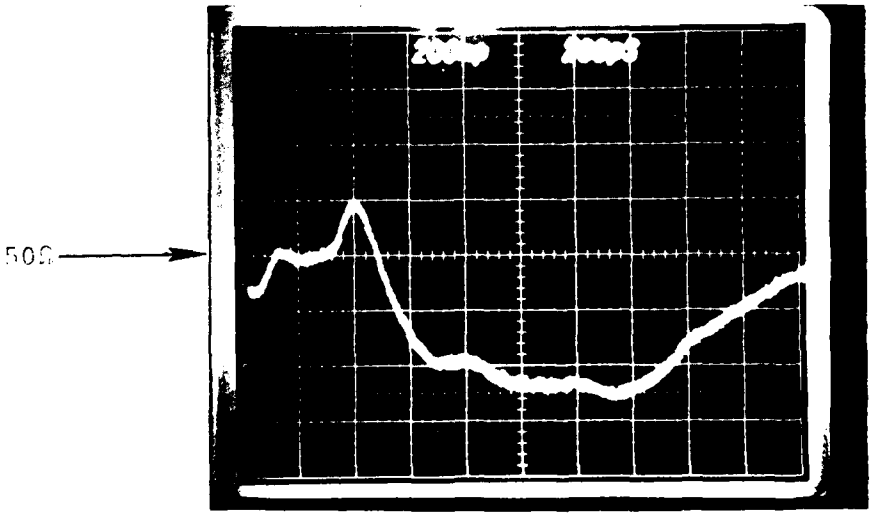

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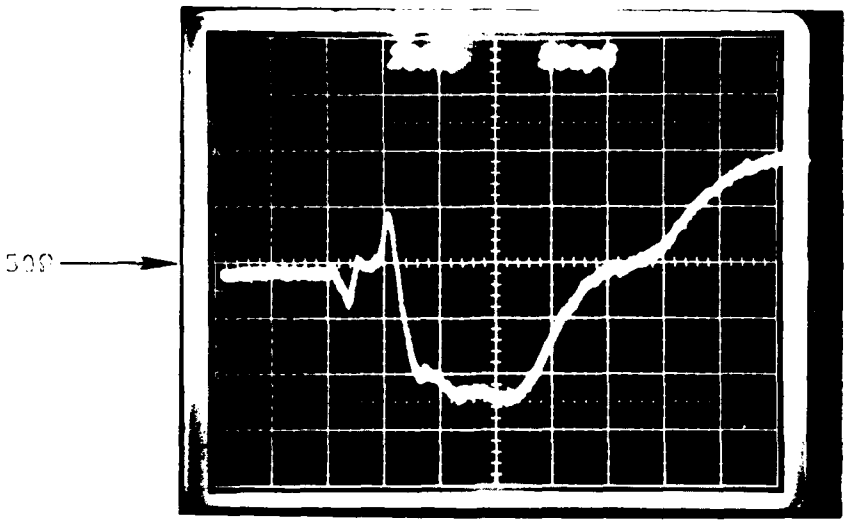

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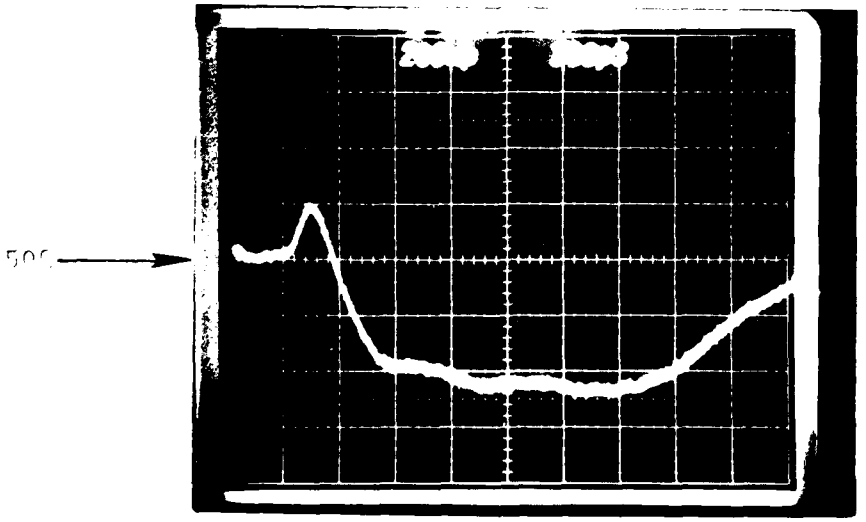

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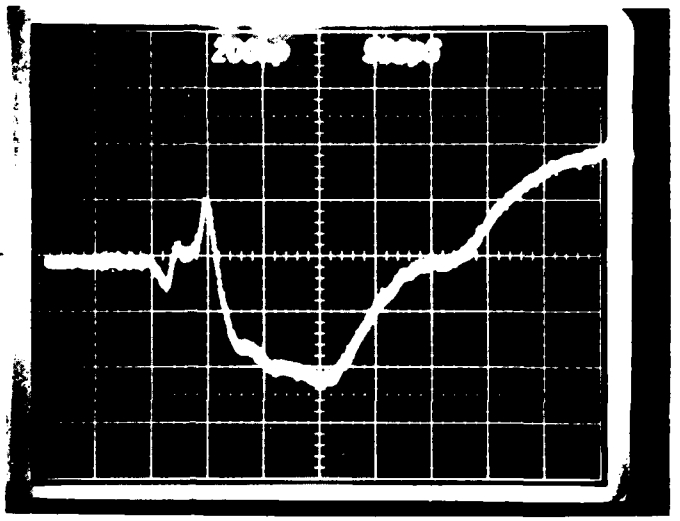


Figure A33 - Line 11

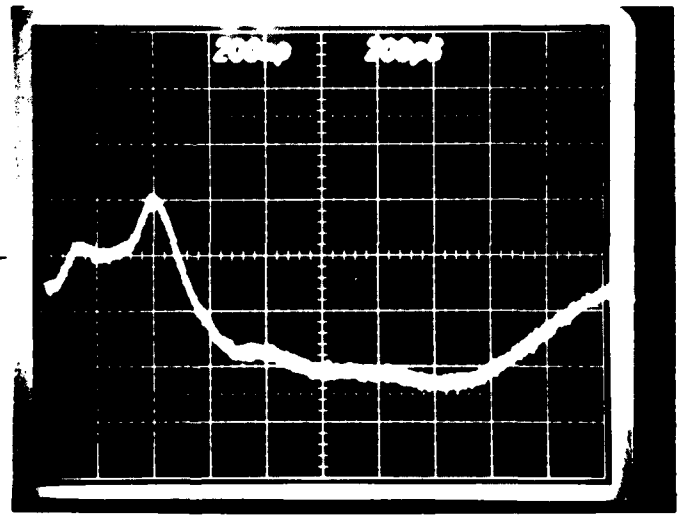
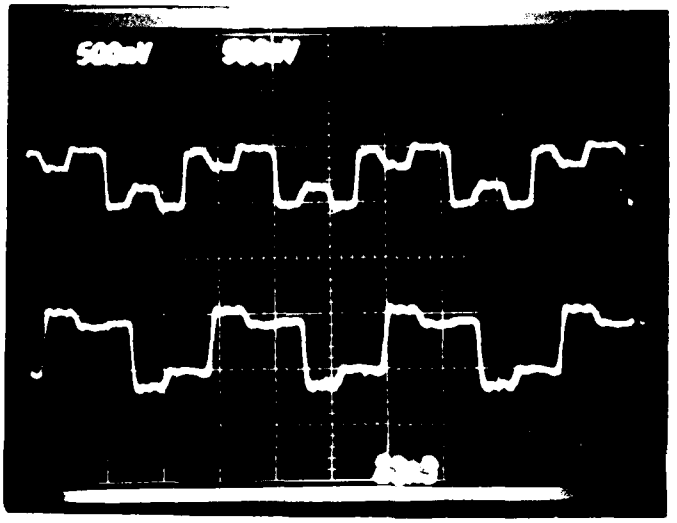


Figure A34 - Line 11

Figure A35 - Line 3



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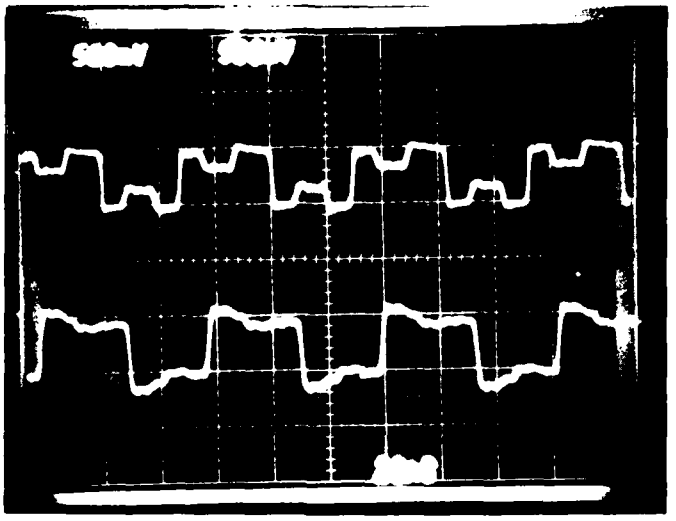
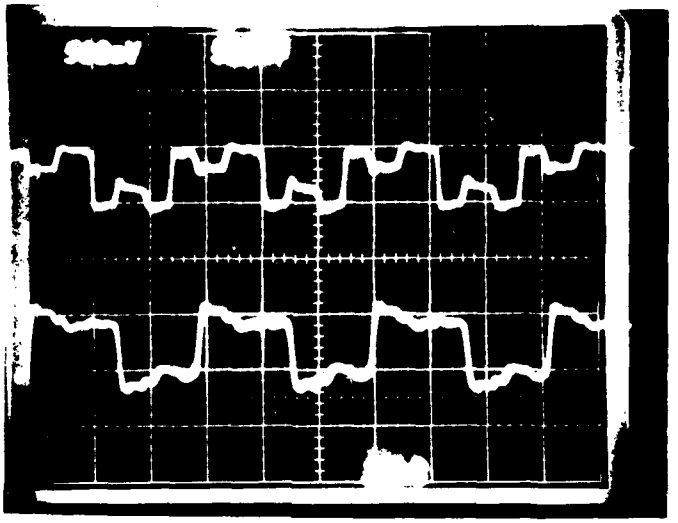


Figure A37 - Line 5

Figure A38 - Line 6

Figure A39 - Line 7

Figure A40 - Line 8



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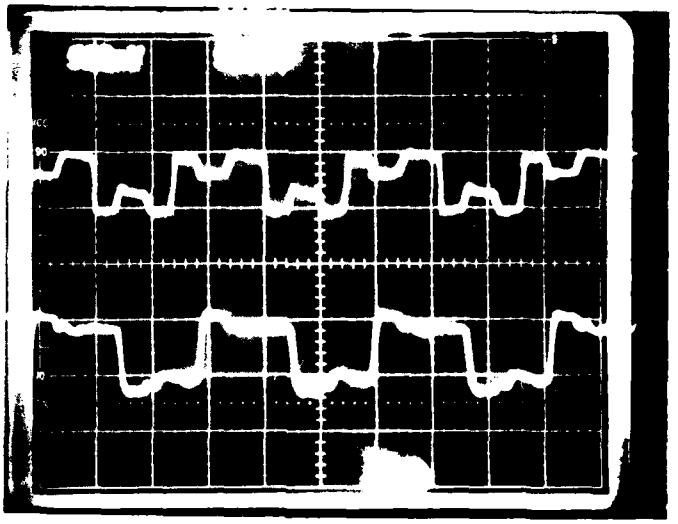


Figure A42 - Line 11

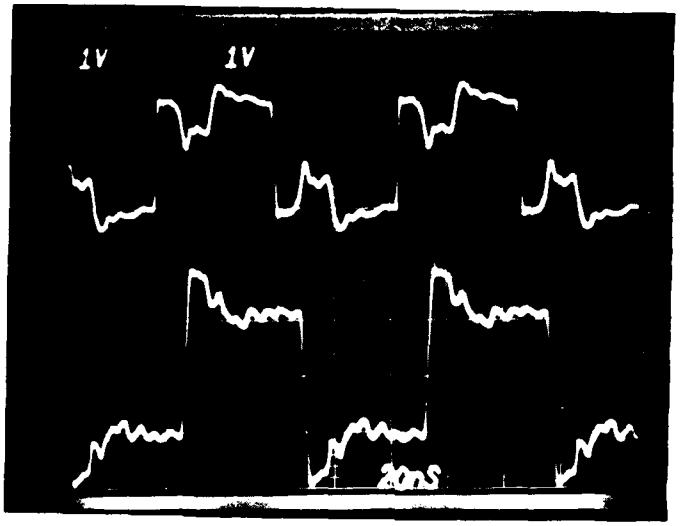


Figure A43 - Line 2 First Layer - Without Second Layer Crossovers

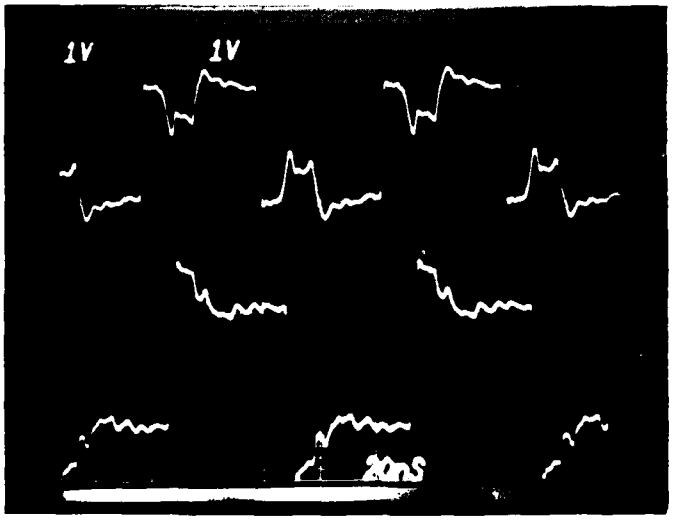


Figure A44 - Line 2 First Layer - With Second Layer Crossovers

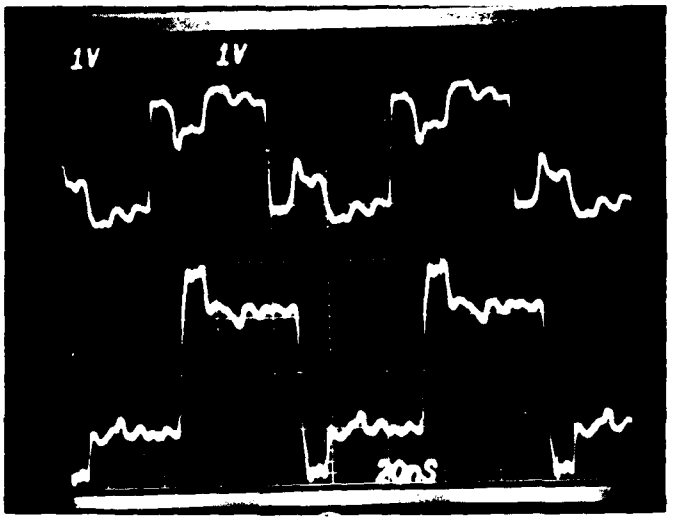


Figure A45 - Line 3 First Layer - Without Second Layer Crossovers

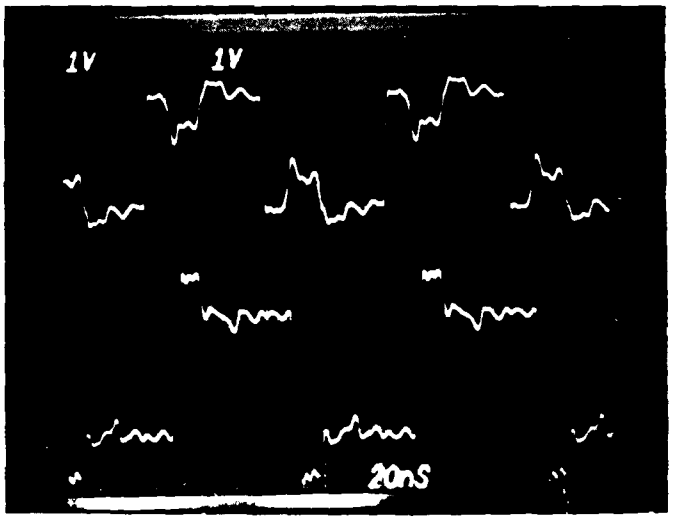


Figure A46 - Line 3 First Layer - With Second Layer Crossovers

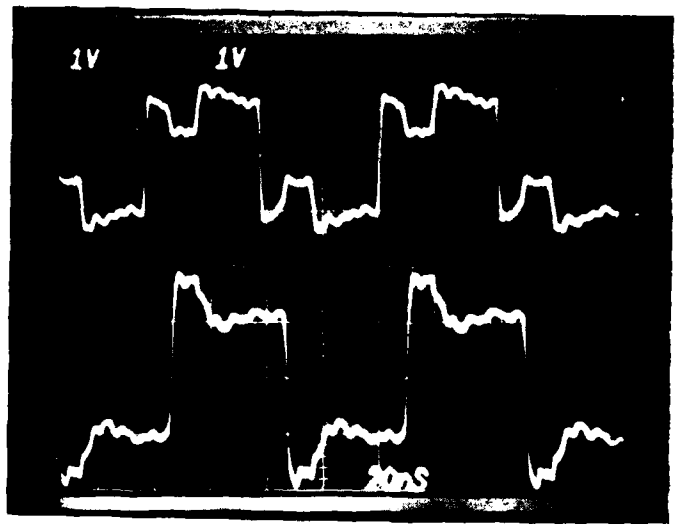


Figure A47 - Line 14 Second Layer

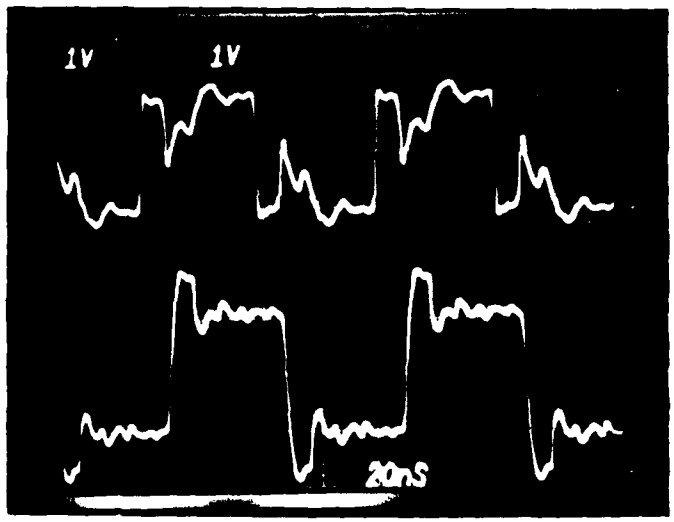


Figure A48 - Line 15 Second Layer - Stripline

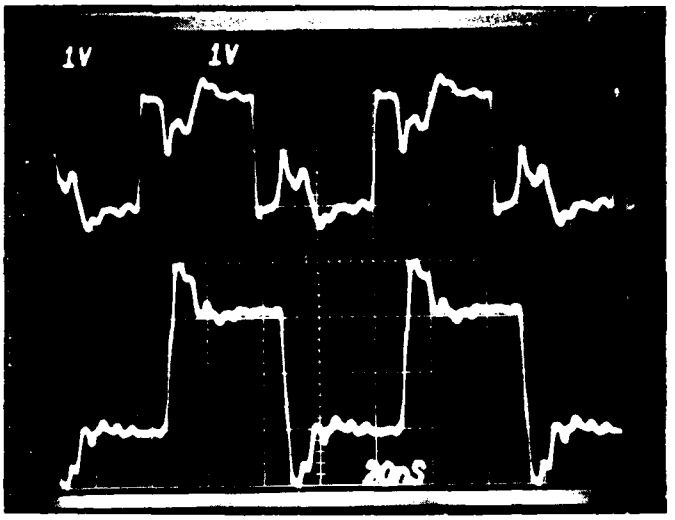


Figure A49 - Line 9 Second Layer - Serpentine - 10 VIAS

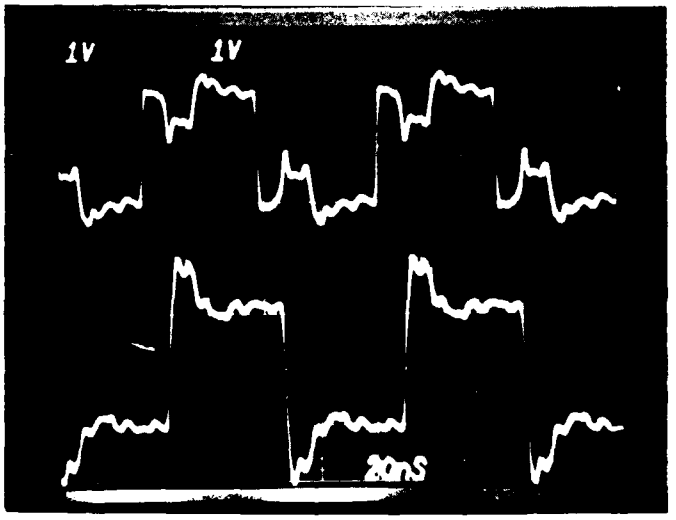


Figure A50 - Line 12 Second Layer - Serpentine - 5 VIAS

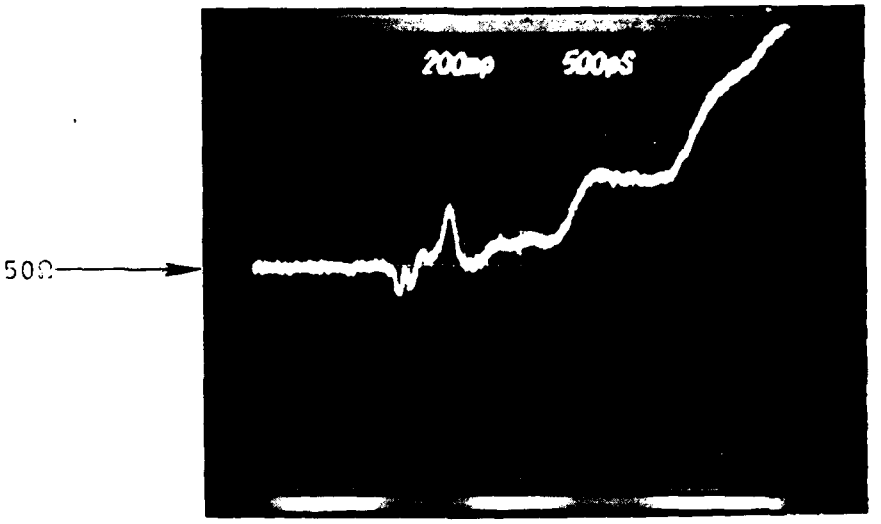
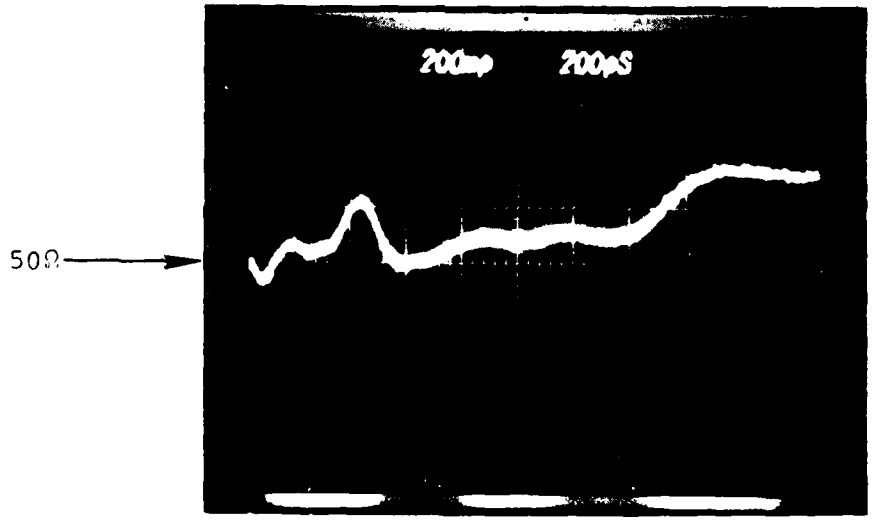


Figure A51 - Line 2



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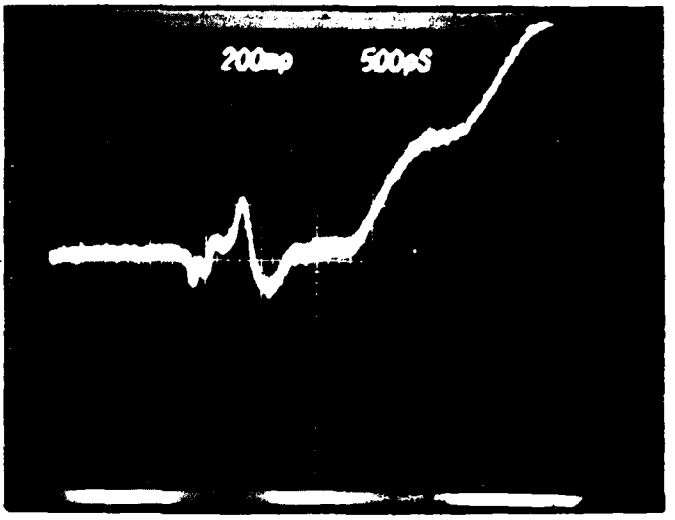

Figure A53 - Line 3

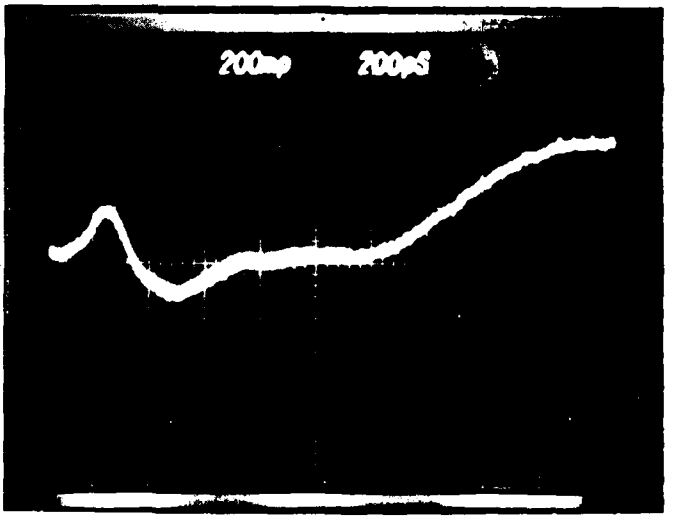

Figure A54 - Line 3

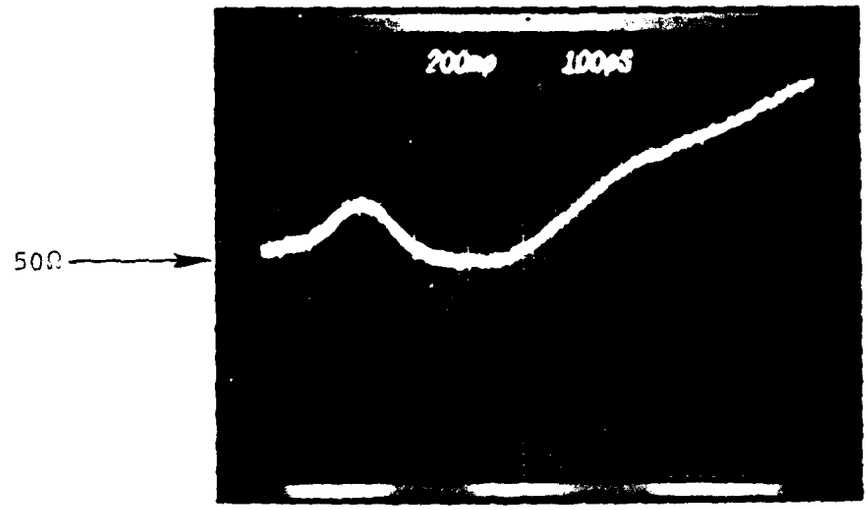

Figure A55 - Line 4

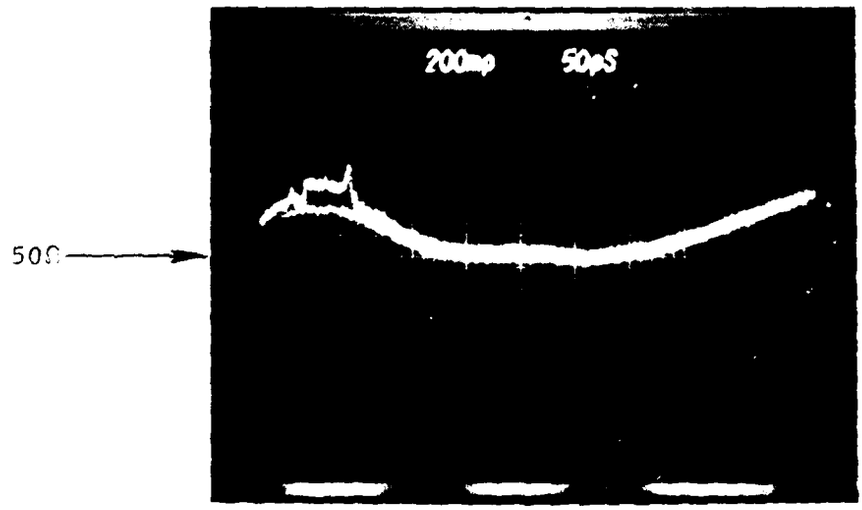

Figure A56 - Line 4

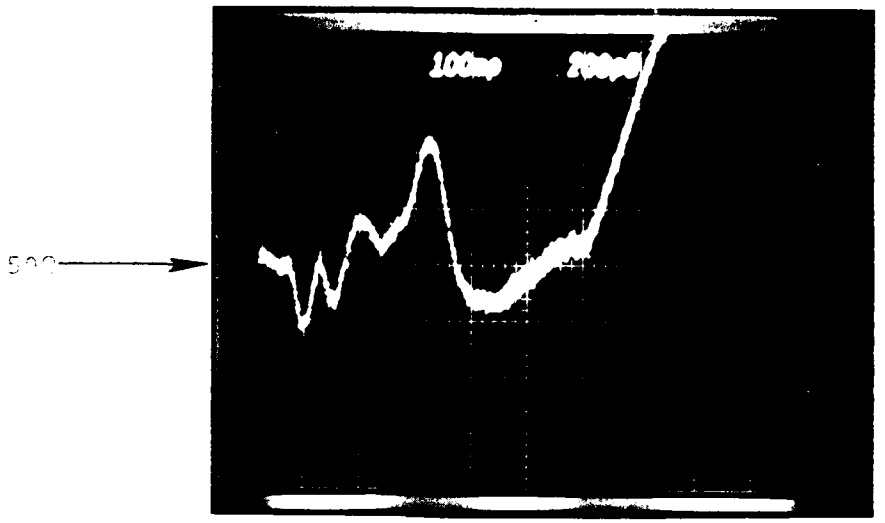

Figure A57 - Line 5

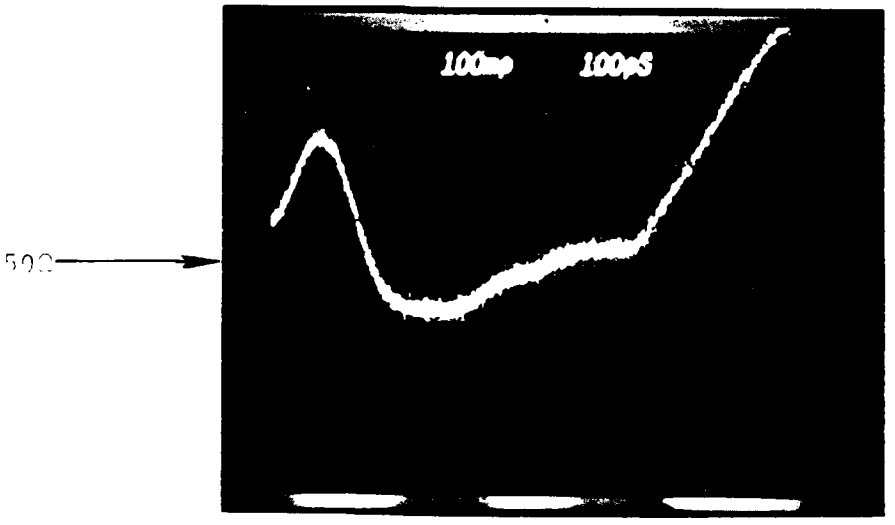

Figure A58 - Line 5

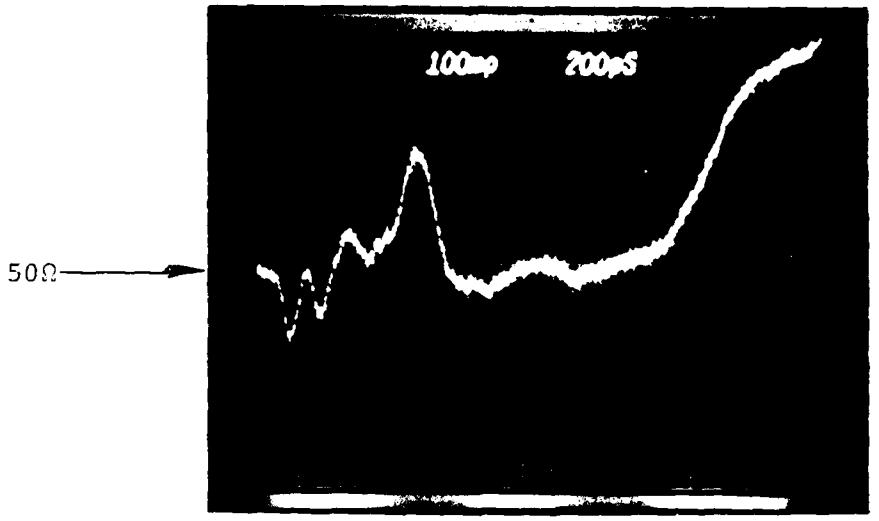

Figure A59 - Line 6

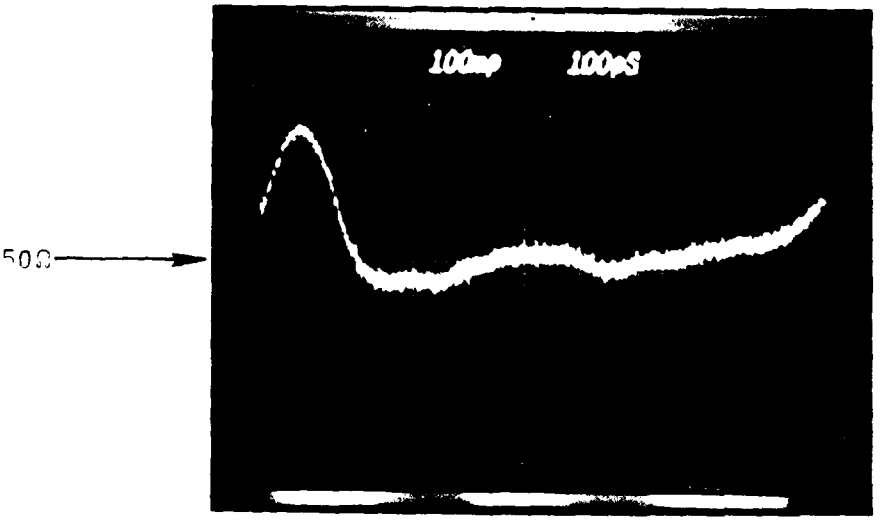

Figure A60 - Line 6

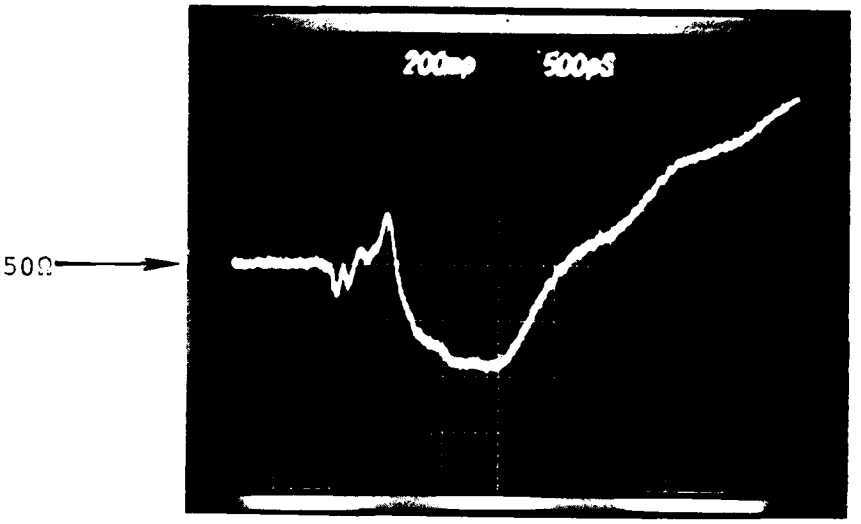

Figure A61 - Line 7

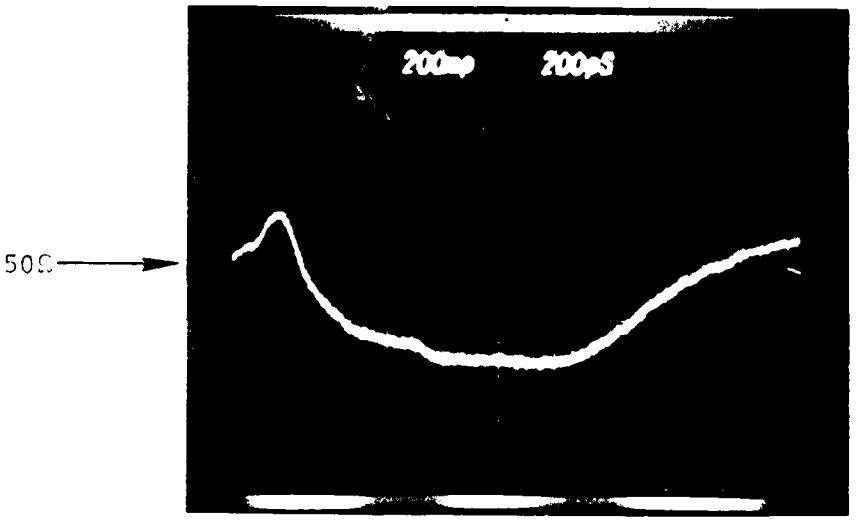

Figure A62 - Line 7

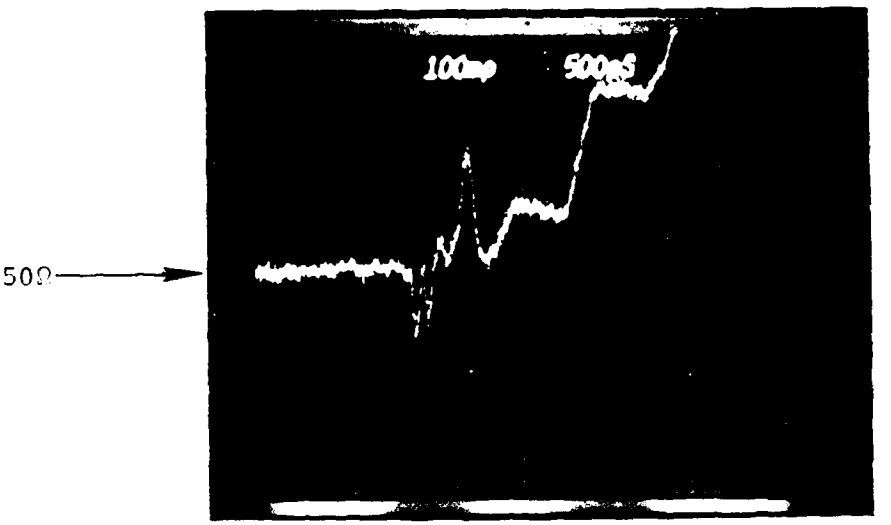

Figure A63 - Line 8

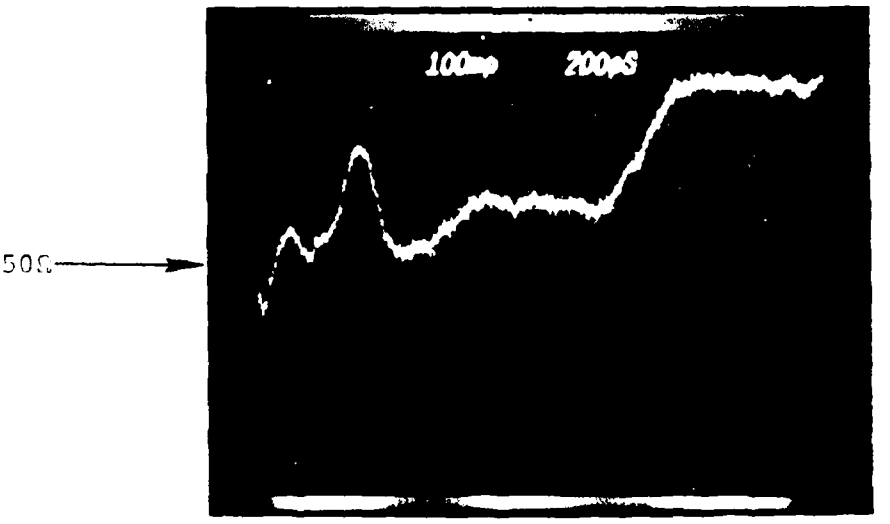

Figure A64 - Line 8

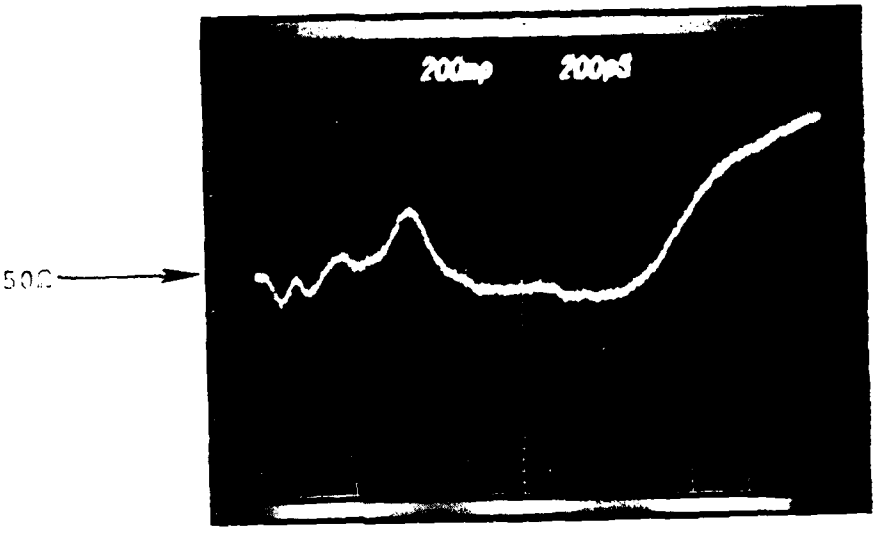

Figure A65 - Line 10

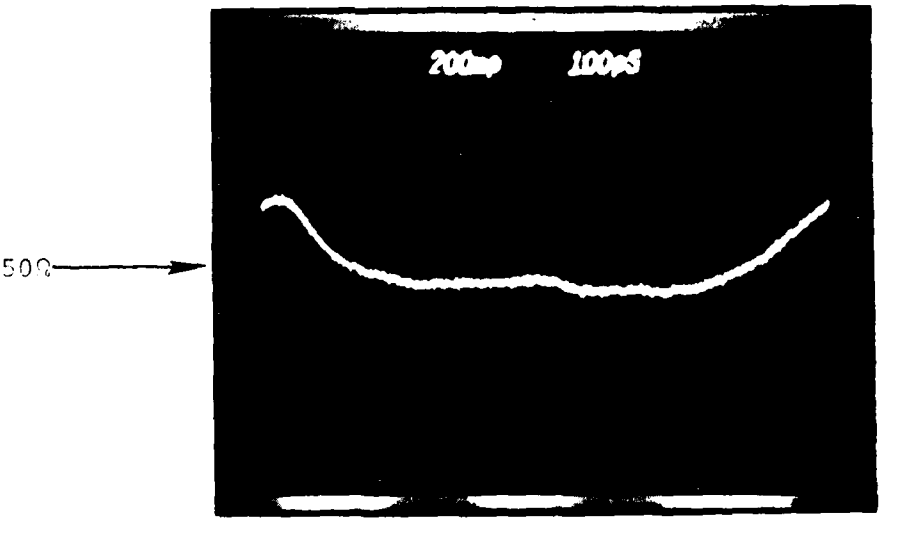

Figure A66 - Line 10

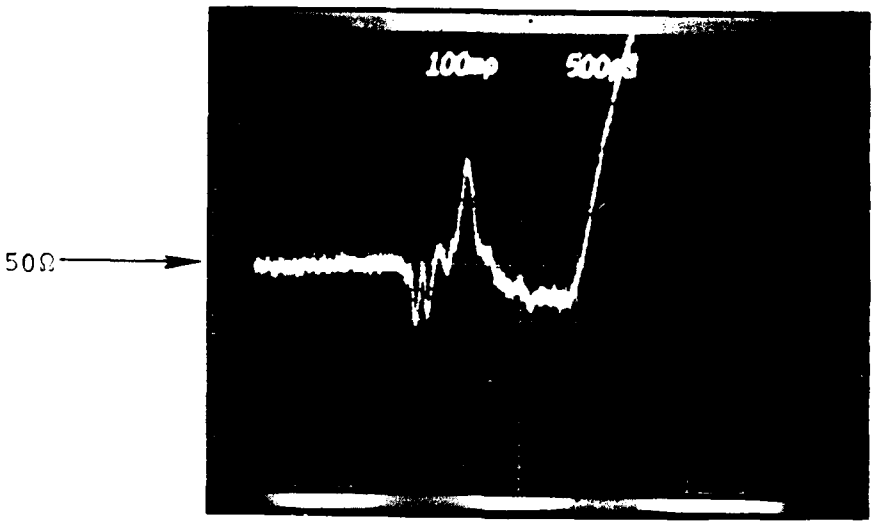

Figure A67 - Line 11

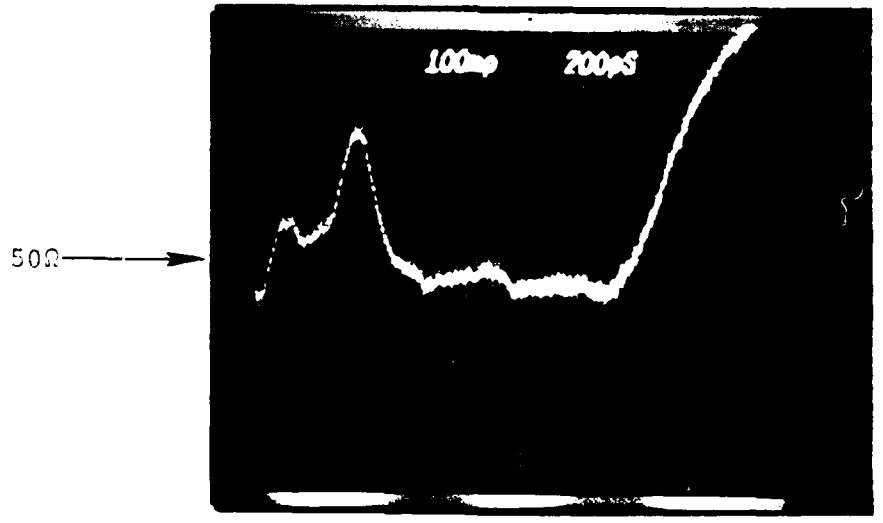

Figure A68 - Line 11

INPUT

OUTPUT

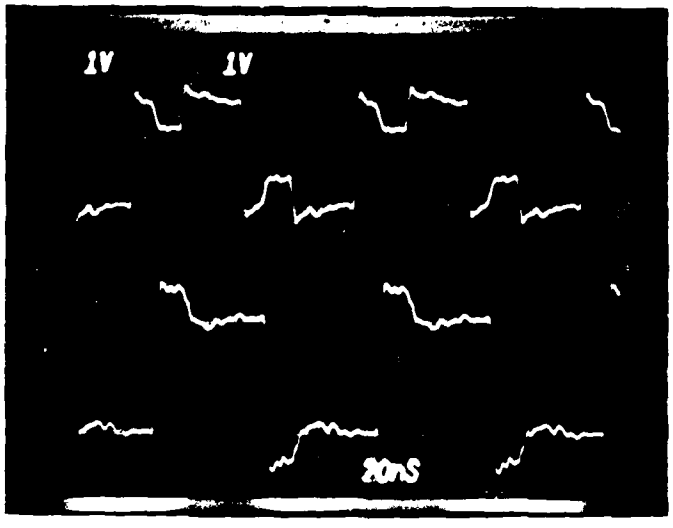

Figure A69 - Line 3

INPUT

OUTPUT

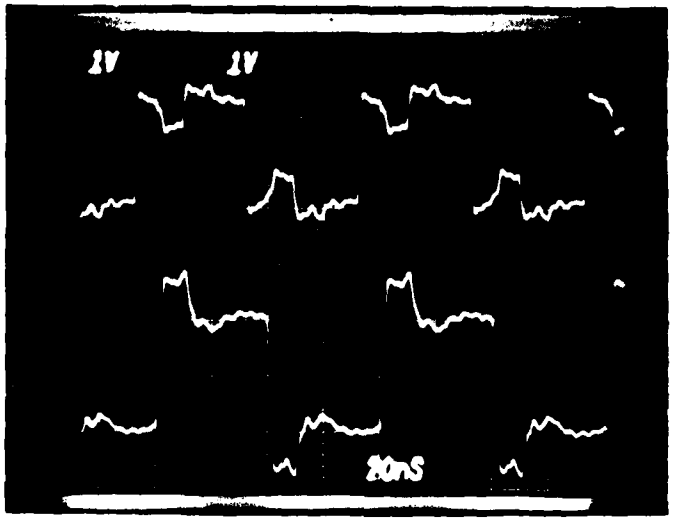

Figure A70 - Line 4

INPUT

OUTPUT

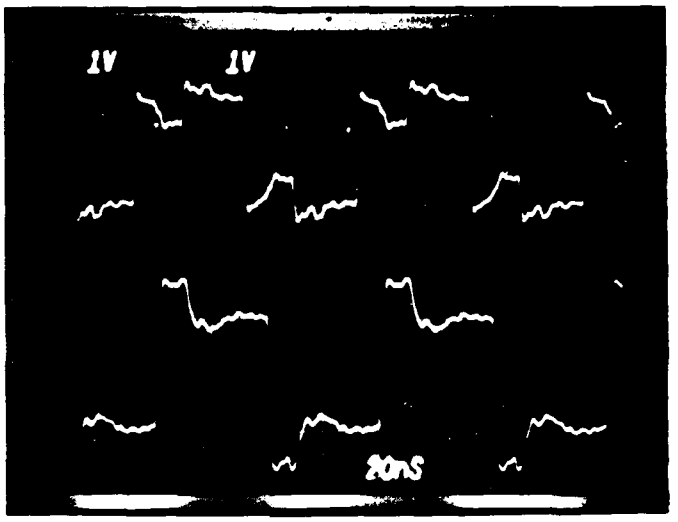

Figure A71 - Line 5

INPUT

OUTPUT

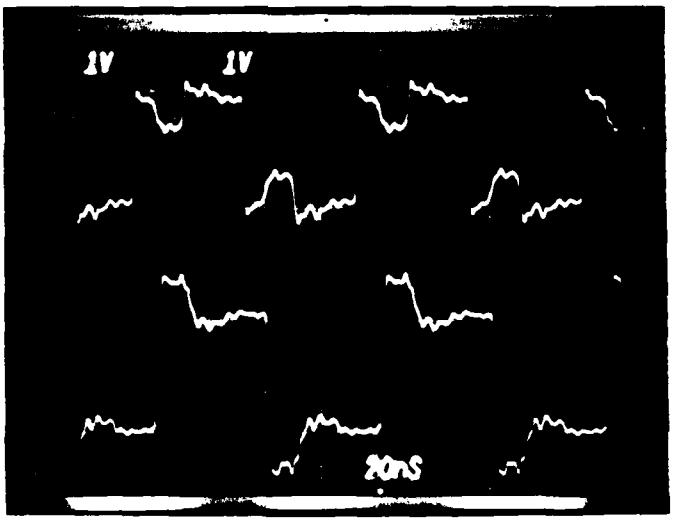

Figure A72 - Line 6

INPUT

OUTPUT

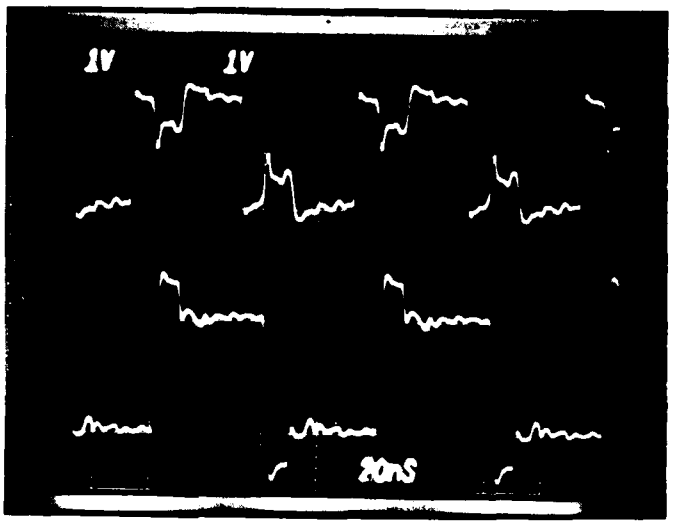

Figure A73 - Line 7

INPUT

OUTPUT

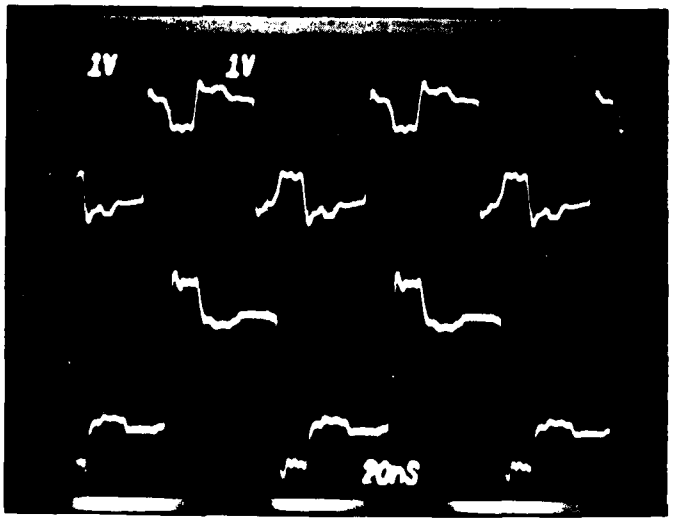

Figure A74 - Line 8

INPUT

OUTPUT

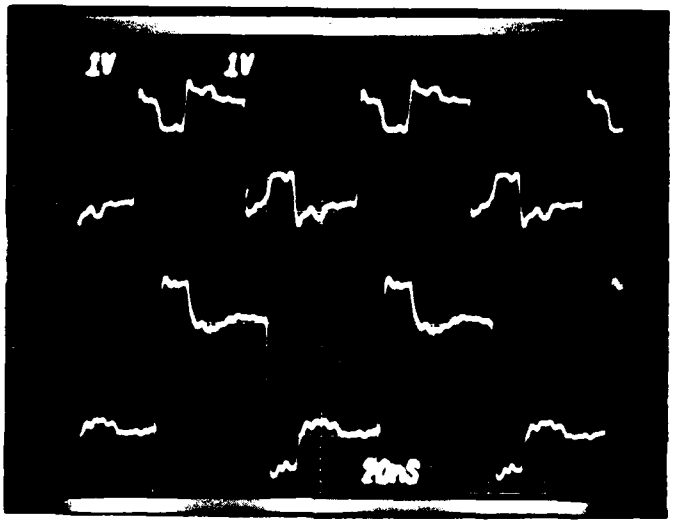

Figure A75 - Line 10

INPUT

OUTPUT

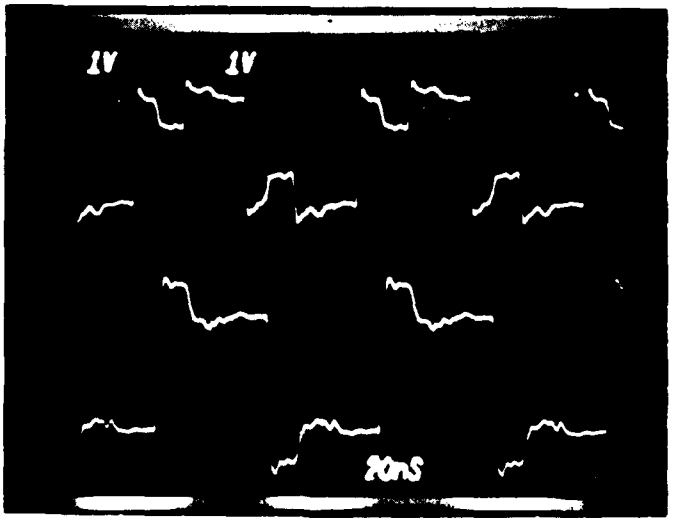

Figure A76 - Line 11

APPENDIX B

CLOCK

BUFFERED
DIVIDE
BY 2

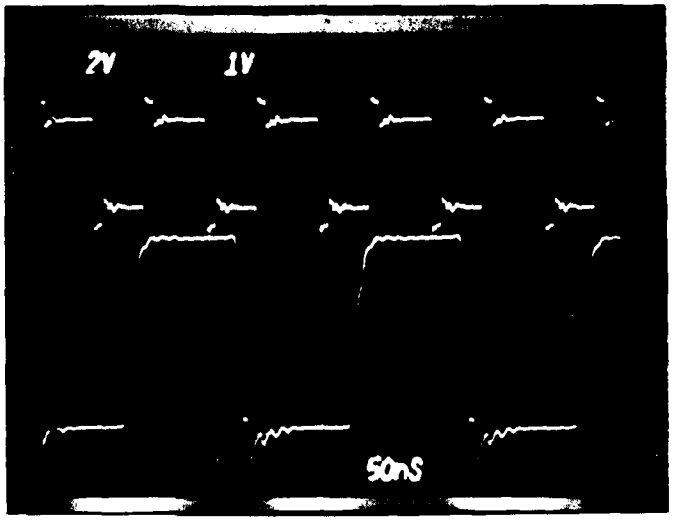

Figure B1 - LSTTL Test Circuit

CLOCK

DIVIDE
BY 4

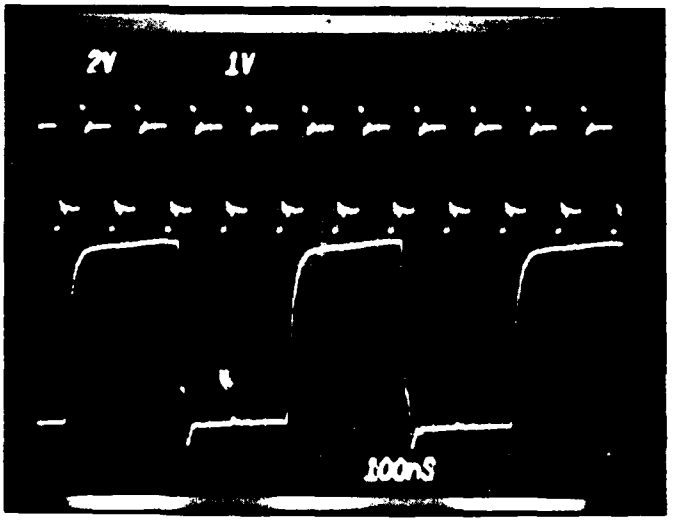

Figure B2 - LSTTL Family

CLOCK

DIVIDE
BY 8

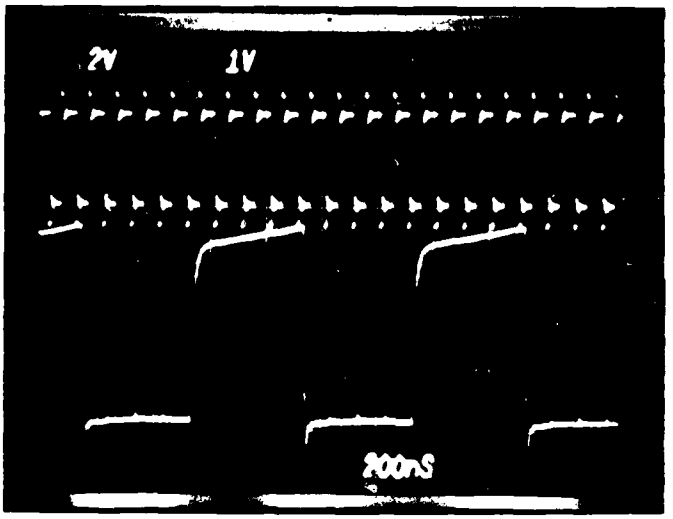

Figure B3 - LSTTL Family

CLOCK

DIVIDE
BY 16

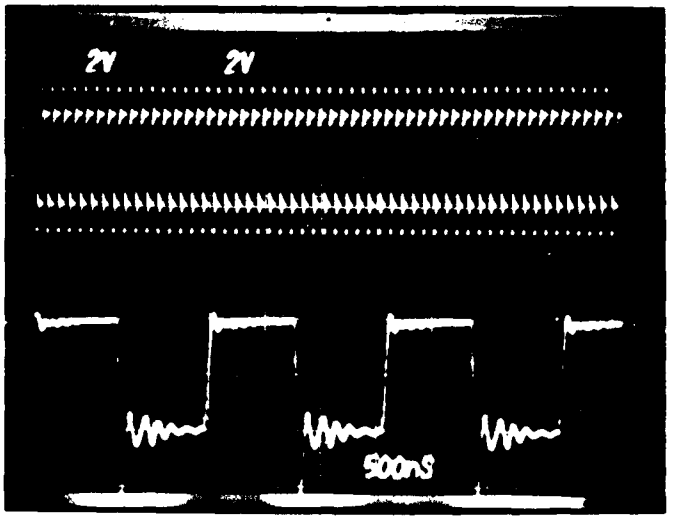

Figure B4 - LSTTL Family

FIRST
GATE INPUT

FIRST
GATE OUTPUT

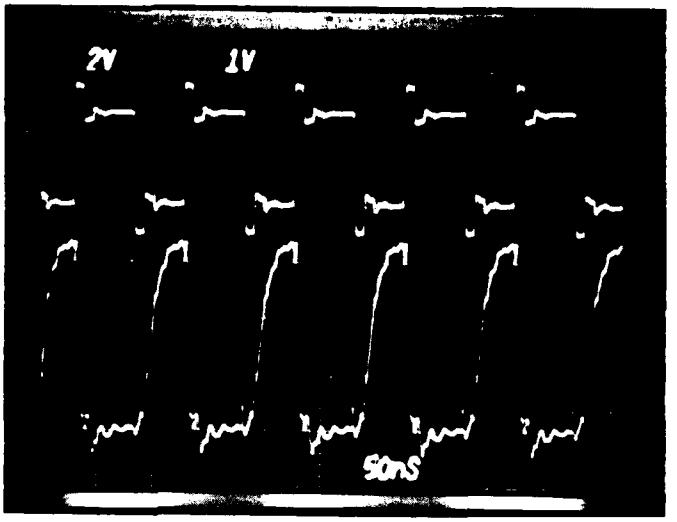

Figure B5 - LSTTL Family

FIRST
GATE INPUT

SECOND
GATE INPUT

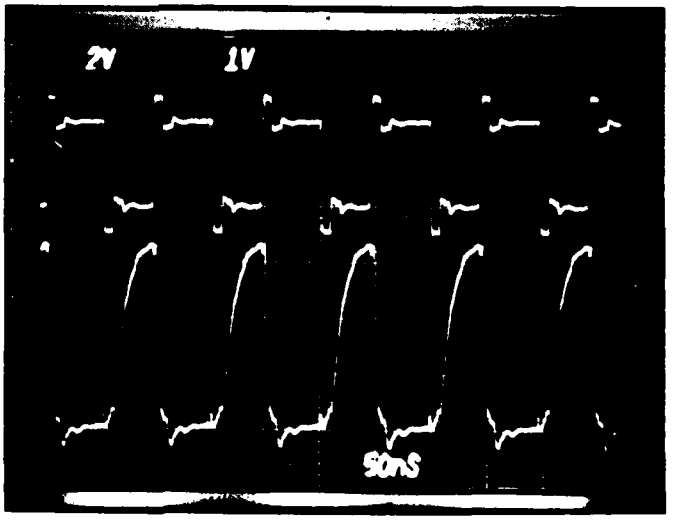

Figure B6 - LSTTL Family

FIRST GATE INPUT

SECOND GATE OUTPUT

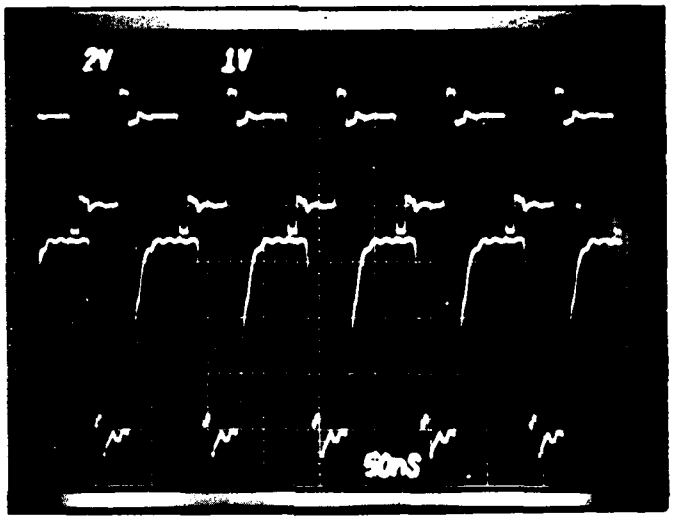

Figure B7 - LSTTL Family

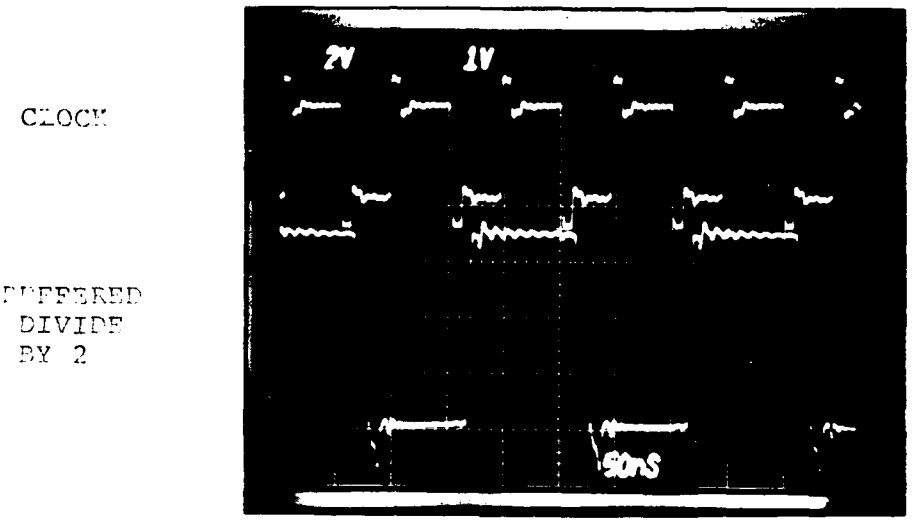

Figure B8 - STTL Family

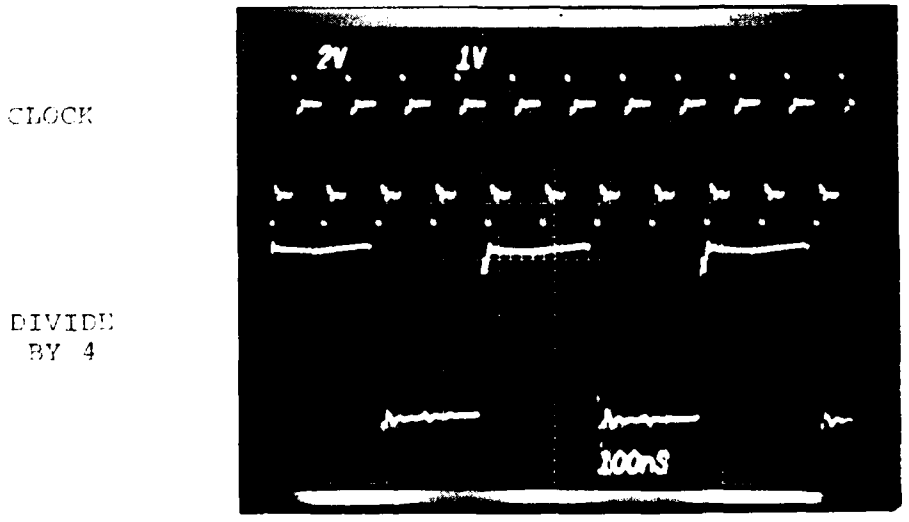

Figure B9 - STTL Family

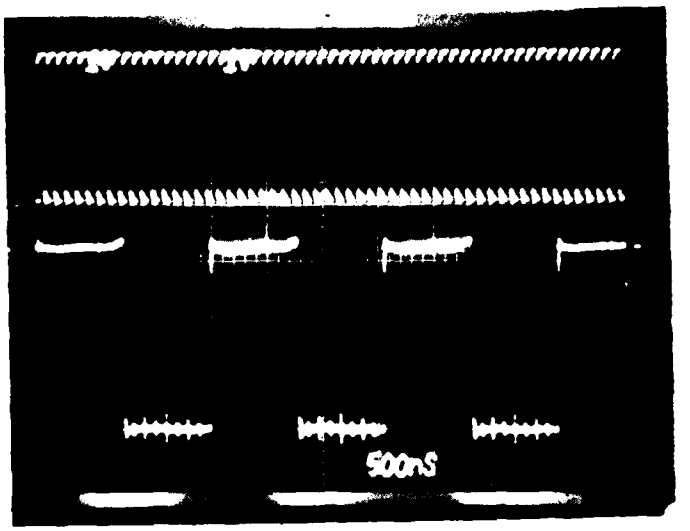

Figure B10 - STTL Family

FIRST GATE
INPUT

FIRST GATE
OUTPUT

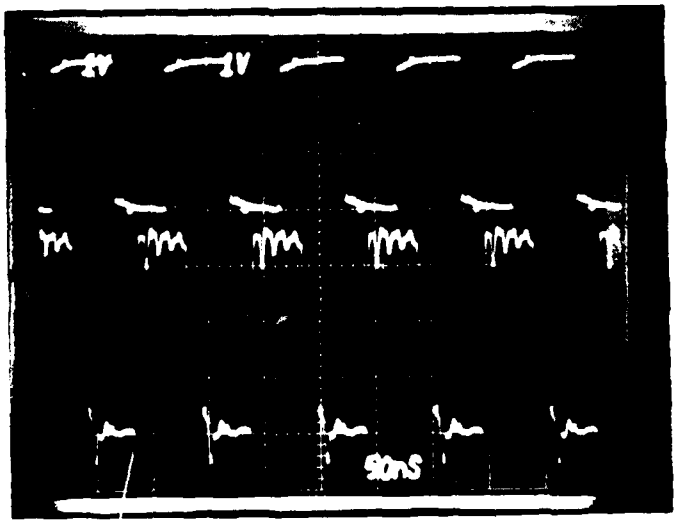

Figure B11 - STTL Family

FIRST GATE
INPUT

SECOND GATE
INPUT

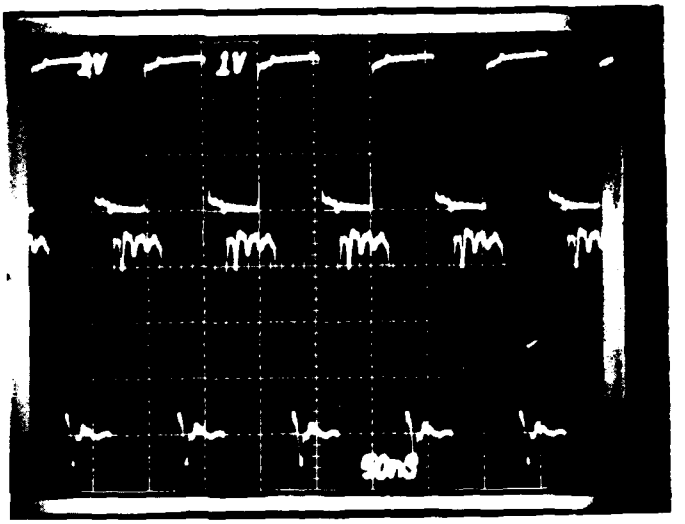

Figure B12 - STTL Family

FIRST GATE
INPUT

SECOND GATE
OUTPUT

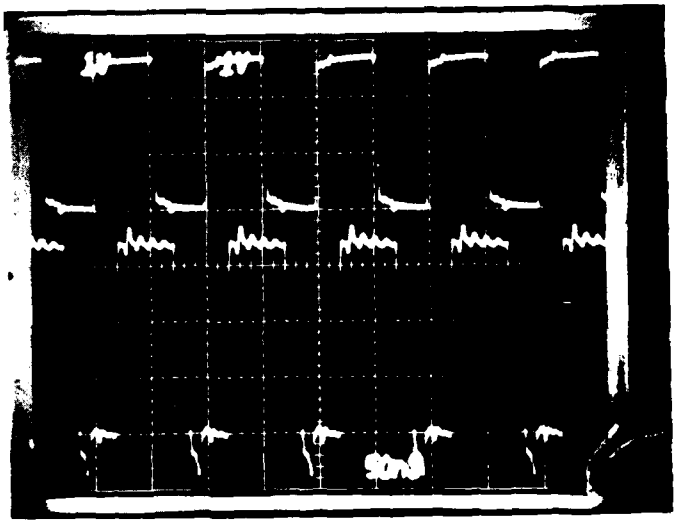

Figure B13 - STTL Family

CLOCK

BUFFERED
DIVIDE
BY 2

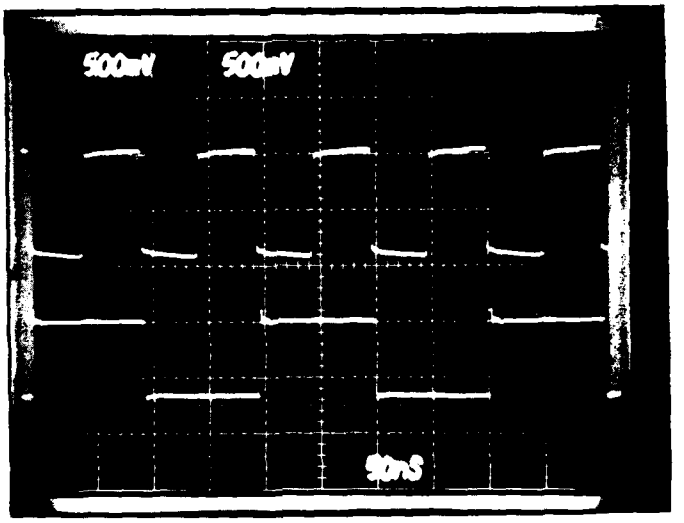

Figure B14 - ECL Family - Counter

FIRST GATE
INPUT

FIRST GATE
OUTPUT

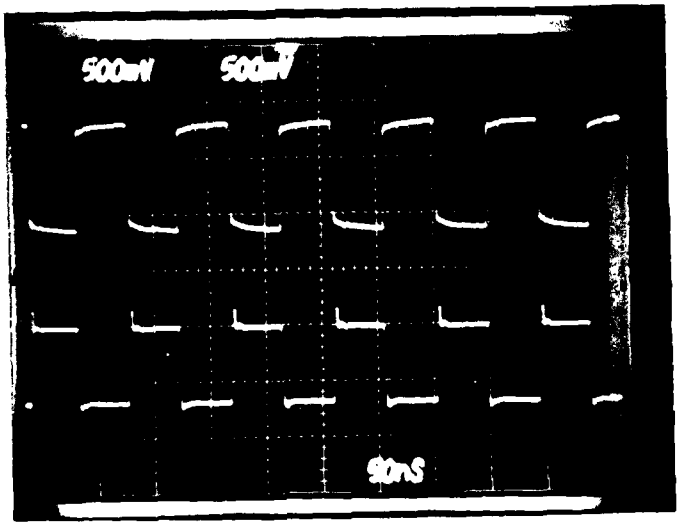

Figure B15 - ECL Family

FIRST GATE
INPUT

SECOND GATE
INPUT

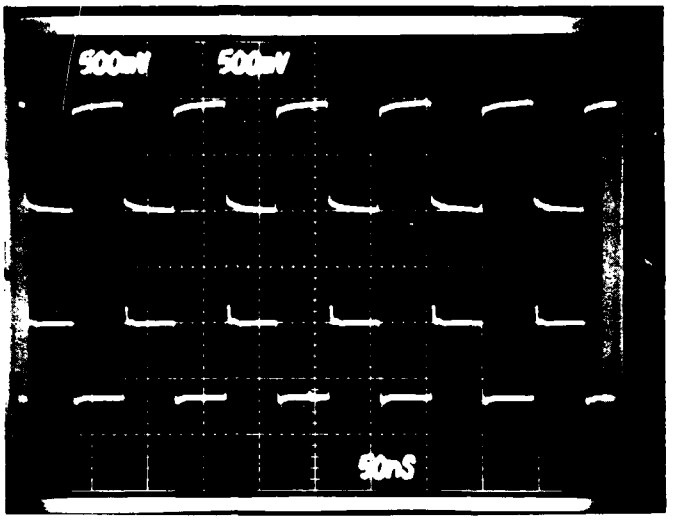

Figure B16 - ECL Family

FIRST GATE
INPUT

SECOND GATE
OUTPUT

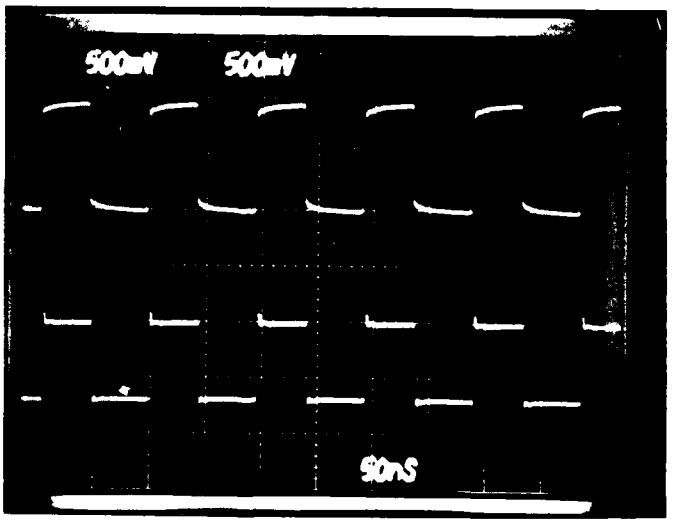

Figure B17 - ECL Family


DAT
ILM